X-743-78-30

THE SOUNDING ROCKET DIVISION AIRBORNE PCM SYSTEM

M. C. ACUÑA, P. L. HINDS,
R. J. STATTEL, R. T. CANNON
AND J. K. NISWANDER

APRIL 1979

NASA
National Aeronautics and
Space Administration

Goddard Space Flight Center
Greenbelt, Maryland 20771

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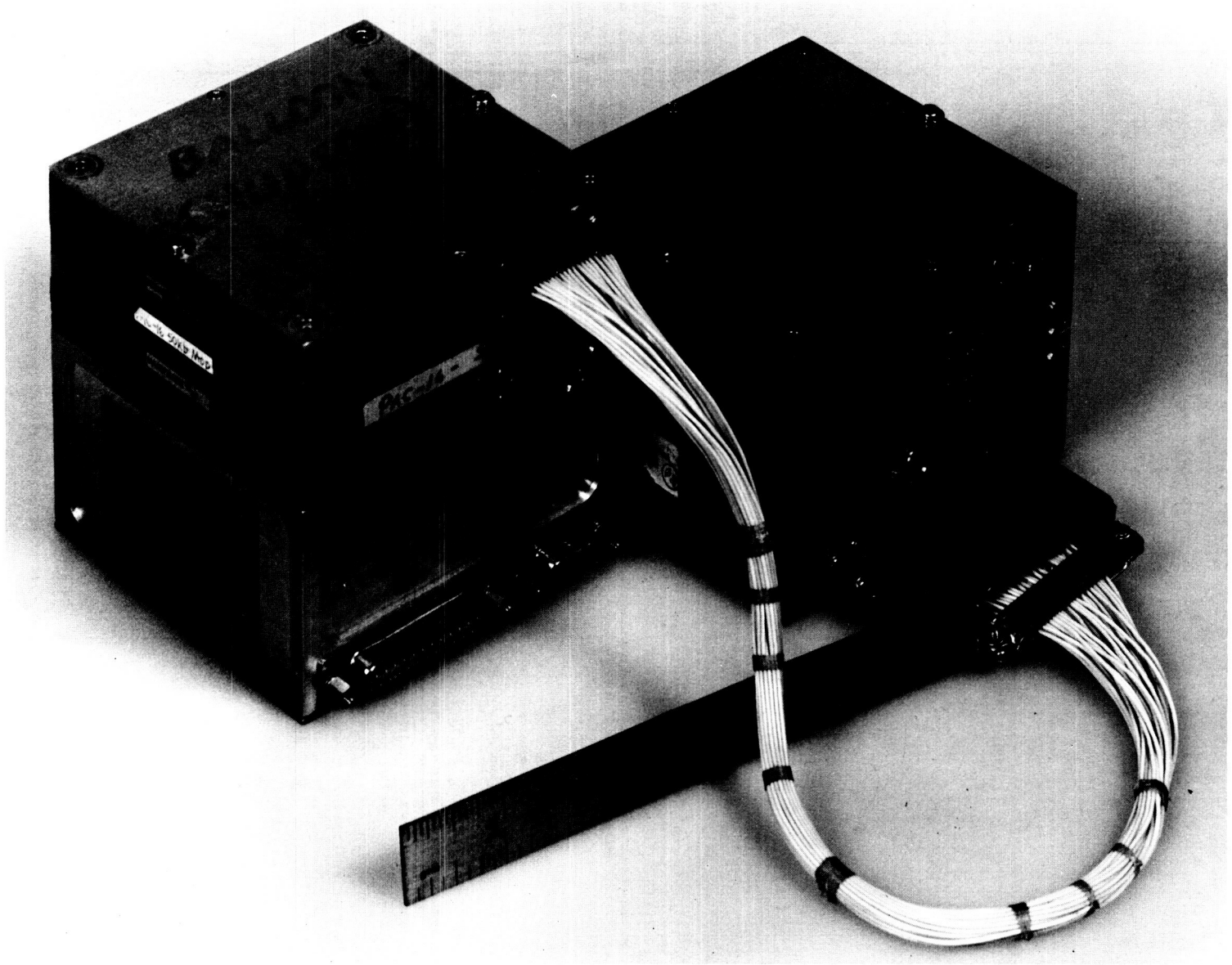

Frontispiece. A Sample System Stack

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ABSTRACT

A flexible, low cost, self-contained PCM encoder system capable of processing up to 448 data inputs is described. The modular construction of the system allows it to efficiently process a small number of analog inputs or be expanded in steps to handle a large variety of data including analog, serial digital, parallel digital, count accumulations, high resolution time-event monitors, etc. The use of an EPROM (electronically programmable read-only memory) yields a system that can be tailored to the experimenter's needs without rewiring and which can be responsive to last-minute field changes, also without rewiring. The flexibility, relatively low cost, modularity and moderate size make the system ideal for a broad range of applications including rockets, balloons, aircraft, shuttle free-flyers, etc.

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GLOSSARY

A/D	Analog to Digital
ADC	Analog to Digital Converter
Bi-Ø-L	Bi-Phase-Level
BPS	(1) Booster Power Supply
	(2) Bits Per Second
D/A	Digital to Analog
DAC	Digital to Analog Converter
LSB	Least Significant Bit
MF	Mainframe
MSB	Most Significant Bit
PCM	Pulse Code Modulation
PROM	Programmable Read Only Memory
SRD	Sounding Rocket Division (GSFC-Code 740)
PAD	Programmable Address Decoder
PAC	Programmable Address Converter

THE SOUNDING ROCKET DIVISION
AIRBORNE PCM SYSTEM

1.0 INTRODUCTION

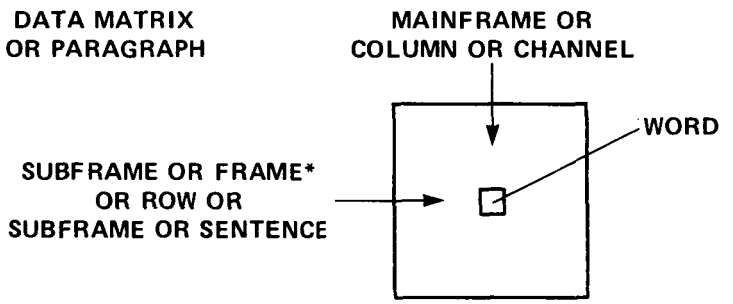
The data collection system described in this report was designed by the Development Section of the Sounding Rocket Instrumentation Branch. The primary goal of the design was flexibility through modularity. A system was needed which would meet the requirements of an enormous variety of sounding rocket experimenters from throughout the country's scientific community. Known data collection requirements ranged from a few simple analog data transducers up to a large complex requirements for hundreds of data from a variety of transducers (analog, digital, pulses, etc.). The system was designed to provide a low-cost modular approach which would handle all known data requirements and which would, additionally, contain an inherent flexibility of both mechanical and electrical construction which would allow future evolvement of the system to accommodate data collection requirements beyond those specifically known to the system designers during the initial design phase. The design has proven very successful. The system has flown on over a hundred sounding rockets, and several aircraft and balloon payloads since the prototype flight in June of 1972. In December 1973, the system was described in NASA document X-743-73-385 (Sounding Rocket Airborne PCM System), but several modules and an optional 50kbit rate have been added since then and this report is an update of the 1973 document. The case of designing new modules into the system has confirmed the design flexibility.

2.0 GENERAL DESCRIPTION OF THE SYSTEM

The heart of the system, both electrically and mechanically, is the SRT/MF shown in Figure 3.0.1. The SRT/MF is the central data collection and encoding unit. By itself, it can process up to 14 analog inputs brought in through its Cannon connector (see Appendix A).

Add-on data modules have the same mechanical side-dimensions as the SRT/MF and have AUGAT through-pins corresponding to those on the top board of the SRT/MF. The data modules interact with the SRT/MF in much the same way as a micro computer interacts with its peripherals. There is an address bus and a data bus plus control lines, all going up the stack through the AUGAT pins. Each data module has its own input data connector. A complete listing of pin assignments for these connectors is given in Appendix A.

The data inputs are processed into a data matrix format shown in Figure 2.0.2. The matrix is referred to by the following terminology:



An analog input to the SRT/MF would be put into a mainframe (column) of the matrix, except for columns 0 and 1 which are reserved for the sync code and subframe count. The matrix has 512 words, 64 of which (columns 0 and 1) are reserved for sync and subframe count, leaving 448 for data. As will be explained in Section 4.2, these 448 words can be filled from only 256 different inputs but these 256 can be any combination of digital, analog, counts, events, etc. The use of the AUGAT through pins allows any combination of data modules to be stacked in an arbitrary sequence on top of the SRT/MF. The number and type of data modules is determined by the experimenter's data requirements. When the number of modules exceeds the excess capacity of the SRT/MF power supply, a new stack can be started on top of a booster power supply (BPS-5). A fairly large such system is illustrated in the frontispiece of this report.

The format of the data – that is, the relationship between the experimenter's data inputs and their position in the paragraph, is determined completely by a programmable address converter (PAC-16) in conjunction with the priority scheme and common bus structure of the system. There has been some confusion about this in the past, thus the following statement:

> The PAC-16 can put any data input to any data module into absolutely any combination of words in the matrix.

*frame is the general term for rows; when discussing a specific row, it would normally be referred to as a subframe and by number (the 17th frame in the matrix is called subframe 17)

It should be noted that this complete freedom of assignment could be used to make assignments which would make absolutely no sense in terms of data sampling theory. The ground support equipment (see Chapter 8) does not allow this degree of freedom and thus is not able to strip out single data values which have been assigned to the matrix at anything other than uniform sampling rates.

The current inventory of data modules includes 32-channel analog multiplexors, serial digital data loaders, pulse-input count accumulators, high-resolution time-event monitors and parallel input data loaders. There are three other modules in the system which do not collect data but which are used for other purposes. These are the programmable address converter, the booster power supply and the signal buffer. The following is a list of all available modules showing the name, type, description, and nominal price (as of March 1979) for each:

Nominal Price	Name	Type	Description
$3,000	SRT/MF	Mainframe	Encoder & ADC
$ 400	PAC-16	Special	Programmable address converter
$ 600	AS-32	Analog	Analog mux
$1,200	ASC-32	Analog	Analog mux with calibrator & event monitors
$ 900	RCM-4	Digital	Count accumulator
(note 1)	SIDL-8	Digital	Serial input data loader
$ 900	SIDL-16	Digital	Serial input data loader
$1,000	TEM-4	Digital	Time event monitor
$1,600	RBM-4	Digital	Remote parallel data loader
$ 250	BUF-4	Digital	Signal buffer to experimenter
$1,300	BPS-5	Special	Booster power supply

The electrical organization of the system is shown in Figure 2.0.1. The only limitations on the mechanical arrangements of the stack are as follows:

1. The SRT/MF always goes on the bottom.

2. The ASC-32 is normally put below the PAC-16 because it is hardwired for channel 15 and the ground station expects the CAL signal to be on 15-31-5.

3. The BUF-4 must go below the PAC-16 so that the address lines coming out will be the real addresses and not those put out by the PAC-16.

4. The TEM-4 must go below the PAC-16 because it must read the true addresses and not the arbitrary ones put out by the PAC-16.

Note 1: SIDL-8 modules are currently in stock but are no longer being purchased, having been replaced by the SIDL-16

The "analog inhibit" and "A/D inhibit" signals are used to give a priority to the system as follows:

Highest priority:	Digital modules
Middle priority:	Analog modules
Lowest priority:	SRT/MF analog

The SRT/MF above automatically puts analog signals into the A/D converter, which then puts its digital output onto the digital data bus. When an analog module is plugged in it uses the "analog inhibit" signal to block off the SRT/MF analog inputs during the time it (the analog module) is being addressed. The A/D output goes to the digital bus but now its analog input is from the analog module rather than from the SRT/MF. When a digital module is plugged in and addressed, it uses the "A/D inhibit" line to block the digital output of the ADC from going onto the digital bus and instead, it (the digital module) puts its data directly onto the digital bus. A simplified block-logic diagram of the priority structure is shown in Figure 2.0.3. The digital bus feeds the pulse-code modulator (parallel to serial converter) in the SRT/MF where the data is converted to PCM serial Bi-Ø-L (Bi-Phase-Level) for transmission.

This section has given a summary description of the system. In the following sections detailed descriptions will be given of the SRT/MF and the various modules.

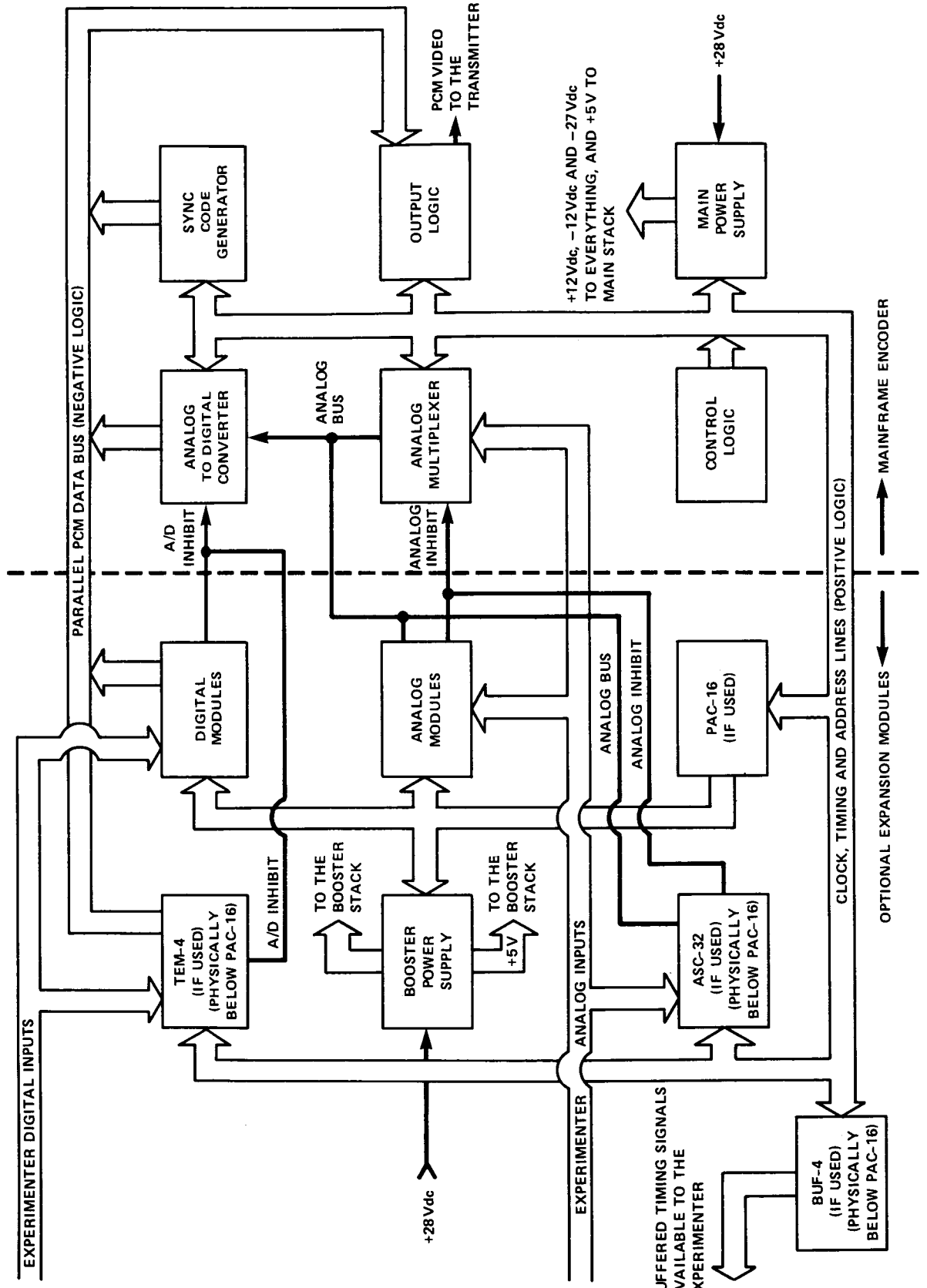


Figure 2.0.1. PCM System Block Diagram

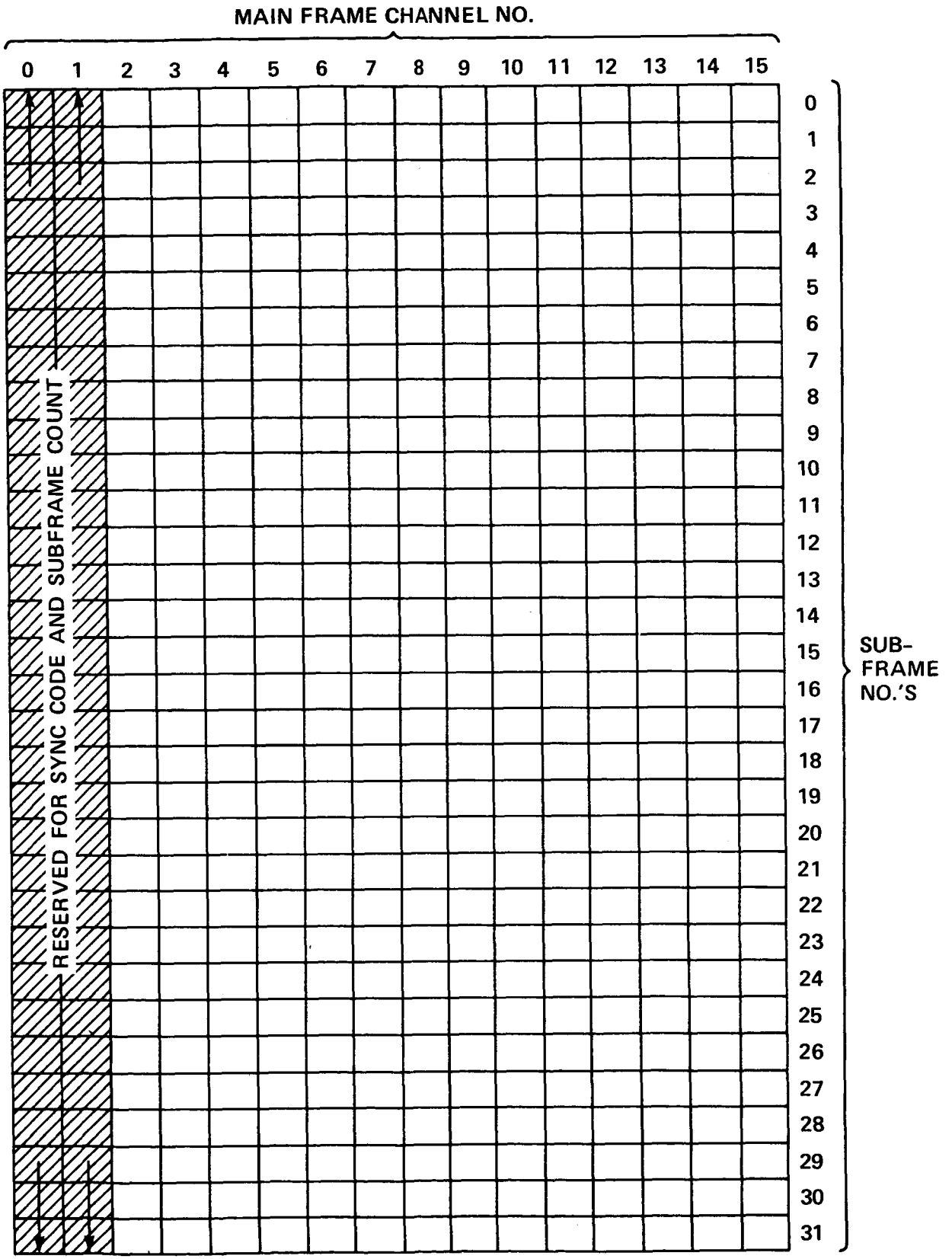


Figure 2.0.2. Data Matrix

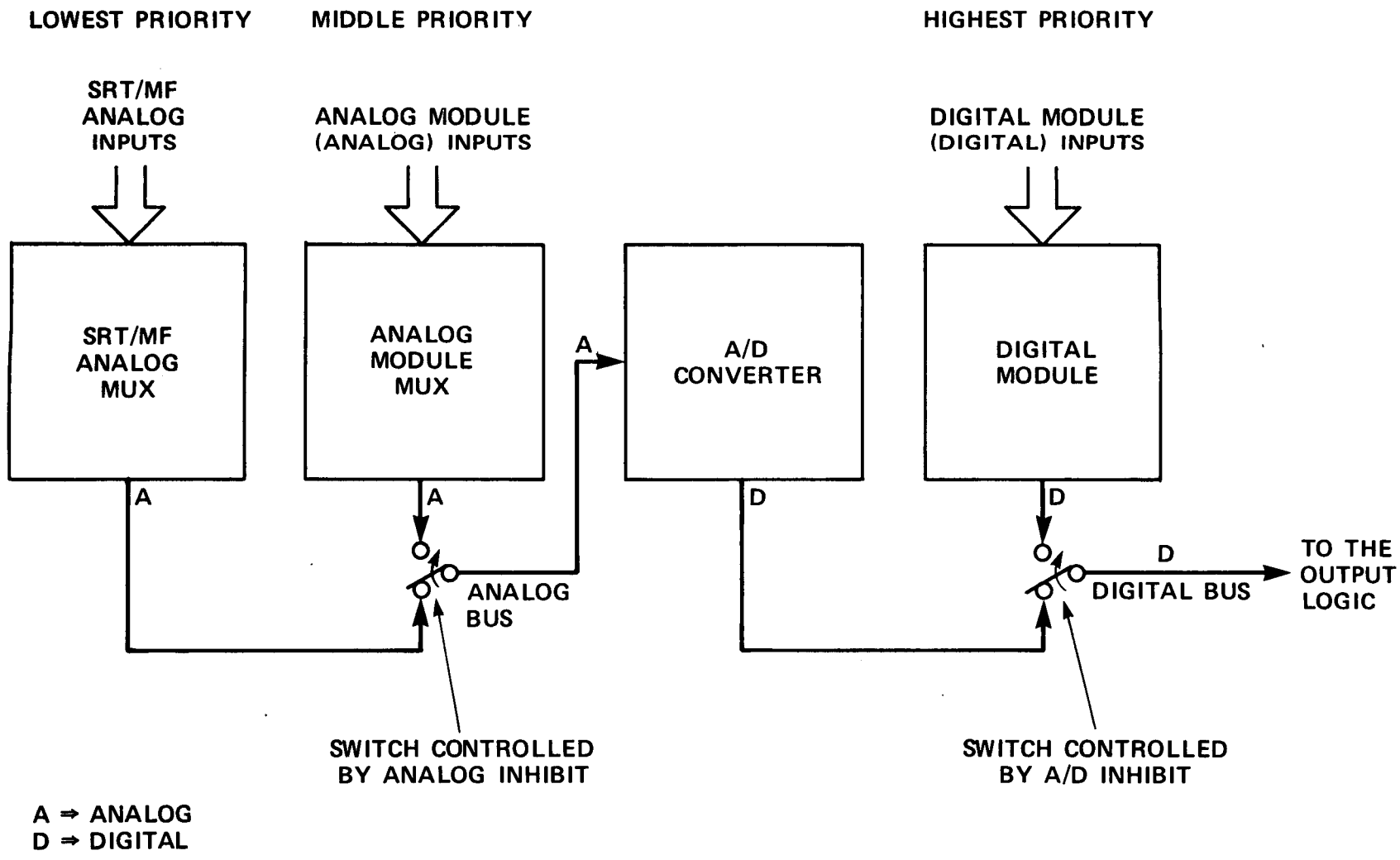


Figure 2.0.3. Priority System Functional Block Diagram

3.0 SRT/MF (Mainframe Encoder)

The SRT/MF can be broken into 6 logical groups of sub-circuits, as shown in Figure 2.0.1. This section will give an overview of the interrelationship of these 6 sub-circuits, and following sections will treat each sub-circuit in detail. An overall understanding of the SRT/MF can best be gained by considering the 6 sub-circuits starting with the output and moving back to the input.

The output logic is responsible for taking 9-bit parallel data from the digital bus during the beginning of a 50μsec word-time and shifting it out serially through a bi-phase-level encoder with MSB first and LSB last. Odd parity is calculated on the 9 bits and is sent out as the tenth bit following the LSB of the data. The data present on the digital bus is put there by one of three sources; the sync code generator, the ADC, or a digital data module.

All data is put onto the digital bus by means of open-collector data transfer gates. The sync code generator puts data on the digital bus during channels 0 and 1. This information is used by the ground station to help reconstruct the data matrix. The digital modules put their data directly onto the bus during whatever channels they are addressed. The priority structure (see Section 2) assures that digital modules will have access to the bus whenever they need it (except during channels 0 and 1). The ADC puts its output on the digital bus when there is no overriding digital module using the bus (and the ADC is also blocked during channels 0 and 1). The ADC input may be from the SRT/MF analog mux or it may be from an analog module, depending on what data is being addressed.

Because the actual process of A/D conversion requires many microseconds (details in Section 3) it is necessary to perform the conversion during the 50μsec word-time prior to the word during which the data is to be output. Collection of serial digital data through a SIDL requires the same advance processing of the data. This means that the data addresses for such data must actually be recognized one word in advance. If an analog data value is to be put out during word #3, for example, then it is necessary that the data be put into the ADC during word #2 so that it will be fully processed into 9-bit binary in time to be dumped onto the digital data bus at the start of word #3 so that it can be shifted out of the output logic during word #3. Similarly, a SIDL which is to put out its data during channel 3 must do its own input shifting during channel 2 so that the accumulated parallel data will be ready by the start of channel 3.

System data other than analog or SIDL data (i.e. data from counters, parallel data, time-events, etc.) do not require advance processing because they are always available in parallel form. However, because of the addressing scheme used, the need for "pre-addressing" the analog and SIDL data necessitates the pre-addressing of all data.

An example:

An analog module is to put out data during channel 3, preceded by a digital data for channel 2. Since the analog module must be addressed during channel 2 in order to provide the necessary pre-processing time, the digital data module cannot be addressed during channel 2 and must therefore be addressed during channel 1.

Therefore, at all times, the address present on the address lines is the address of the word which is to be output during the <u>next</u> 50μsec period, not the current 50μsec period.

The clock, timing, and address lines generated by the control logic are distributed throughout the system. If expansion modules are used, these lines are applied to them. The address lines may be converted by the PAC-16 to any arbitrary value so as to properly address the expansion modules above the PAC. If a large number of expansion modules are used, a booster power supply

may be necessary to augment the SRT/MF power supply. The BPS-5 is transparent as far as the logic of the system is concerned.

To summarize, the SRT/MF consists of the following six functional groups of circuitry.

1. Control Logic	Generates a 512-word matrix format and all required timing lines.
2. Sync Code Generator	Generates a sync code and subframe count into channels 0 and 1 so that the ground stations can reconstruct the data matrix.
3. Analog Multiplexer	Multiplexes one of the 14 analog inputs of the SRT/MF into the ADC.
4. Analog to Digital Converter (ADC)	Converts all system analog inputs into a 9-bit binary word.
5. Output Logic	Converts 9-bit parallel data into a 10-bit, filtered, Bi-Ø-L serial output with odd parity being the 10th bit. Data appears MSB first, parity last.
6. Power Supply	Generates all the power needs of the SRT/MF plus has excess capacity sufficient to drive a number of expansion modules (see Appendix A). Its only input is 28 Vdc.

These six functions will now be discussed in detail.

3.1 Control Logic

The control logic is shown in Figure 3.1. It has an internal 4.0MHz crystal oscillator which is used to generate all of the timing signals for the system. The timing signals are given in Figure 3.0.3.

The output of the 4MHz oscillator is divided by 10, 2 and 10 to generate a 400kHz A/D clock, a 200kHz bit clock, and a 20 kHz word clock. The word clock drives a 4-bit counter to provide the mainframe address lines and the output of this counter in turn drives a 5-bit counter to generate the subframe address lines.

The address lines (mainframe and subframe) constitute a 9-bit binary counter which updates every 50μsec. It should be kept clearly in mind, however, that the address lines coming out of a PAC-16 are dependent entirely on the programming of the PAC's ROM, and that the PAC output lines are therefore arbitrary and not, in a general sense, predictable. For a given PAC programming, of course, the PAC outputs will have a known fixed pattern but a different PAC program may produce a radically different set of outputs.

The control logic's "timing logic" has an array of gates which generate various timing signals during each 50μsec word-time. The data transfer signal is used to strobe digital information (from the sync code generator or a digital module, or the ADC) onto the digital bus for loading into the output logic's shift register. The data reset signal is an auxillary signal available for use by expansion modules; the RCM-4 module can use it to reset counters after their contents have been read out. (This option is not normally used on the RCM's but it is available.) The parity reset

signal is used by the output logic to reset the parity flip flop in preparation for the next word. The A/D converter start signal resets and then starts the ADC.

The data transfer and data reset signals are available throughout the system, including all data modules, but the parity reset and ADC start signals are local to the SRT/MF. The 400kHz A/D clock is available throughout the system and is used for functions other than clocking the ADC. The 200kHz bit clock and the 20kHz word clock are local to the SRT/MF.

The 200kHz bit clock is actually reconstructed in some expansion modules (see SIDL-16) by using the 400kHz clock plus the reset pulse.

3.2 Sync Code Generator

The sync code generator is shown in Figure 3.2. It's purpose is the generation of a 14-bit sync code during channels 0 and 1 of the ground support equipment to reconstruct the data matrix. The 5-bit subframe count is put into word #1 along with the last 4 bits of the sync code. Words 0 and 1 are always as follows:

Word #0	Word #1
1 0 0 1 1 0 0 1 0 1*	1 1 1 1 2^0 2^1 2^2 2^3 2^4 p*
MSB LSB	MSB LSB
*Generated by the parity circuit	Subframe Address

Note that the subframe address bits are in the reverse order from the normal order of data words in that the LSB of the subframe address is transmitted first.

The sync code logic decodes the mainframe address lines to get channel 0 and channel 1 select lines which in turn are used to enable data transfer gates so as to put the sync code and subframe count into the data matrix at the appropriate times. The sync lines are OR'ed to form an A/D inhibit so as to prevent the ADC from accessing the data bus during channels 0 and 1.

Note that since the contents of word #0 never change, the parity bit for the word also never changes and is, in fact, always a 1 and is considered a part of the 14-bit sync code. The parity bit of word #1 will depend on what bits are on in the subframe address.

3.3 Analog Multiplexer

The analog multiplexer is shown in Figure 3.3. It allows analog data to be multiplexed into any of the 14 mainframe data channels. An input protection circuit consisting of diode clamps and a series resistor for each channel protects the MOS multiplexers from over- or reverse-voltage within the range of ±35 Vdc.

The analog mux is not capable of any subcommutation or in fact of any data rate other than one channel per input. Since the system needs subcommutation capabilities for analog signals, analog data modules have been incorporated which can be programmed to any sampling rate. These modules do not contain their own ADC but rather present their analog data to the SRT/MF via the same analog bus as is used by the SRT/MF analog mux. It is necessary to avoid conflicts on the analog bus, and this is done by having the analog data modules send an "analog inhibit" to the SRT/MF analog mux. Thus, at the same time an analog data module is putting its data on the analog bus, it is disconnecting the SRT/MF analog mux from the analog bus.

Because of the time required to perform an analog to digital conversion, the analog data values must be put onto the analog bus one word prior to the time at which they are supposed to appear on the output. A close examination of Figure 3.3 will show that the 14 analog signal inputs (which are labeled according to the number of the word-time during which they are supposed to appear on the output) are actually addressed one word earlier than their output time. For example, the right-most input of the left mux is labeled "8" because it is supposed to come out on the output data stream during channel 8, yet it is clearly addressed when the channel number is 7, thus allowing the A/D converter the necessary time to perform the A/D conversion. Note also that the left-most and right-most mux inputs are grounded. These correspond to output channels 0 and 1 during which time the analog bus is ignored anyway because the sync code generator takes over the digital bus.

3.4 Analog to Digital Converter (ADC)

The ADC section of the SRT/MF is a 9-bit successive approximation A/D converter with an accuracy of 8 bits ±1/2 bit. Zero adjust and gain adjust are provided, as shown in Figure 3.4, and a preflight calibration can increase the effective accuracy to 9 bits ±1/2 bit. In fact, a system in-flight calibration is normally provided by the ASC-32 (see Section 5.2) thus always assuring a 9-bit accuracy (±1/2 bit). Figure 3.0.3 shows the timing of the A/D conversion process. The A/D start command is issued 15 μsec after a word boundary. During the 2.5 μsec duration of the command, the converter's timing and storage sections are reset and the conversion begins at the end of the A/D start command. During the 17.5 μsecs between the word boundary and the end of the A/D start command, the analog signal is input to the ADC on the analog bus and allowed to settle. There is no sample and hold for the analog signal.

The conversion takes place MSB first at a clock rate of 400 kHz. Initially the timing control circuitry forces the storage register MSB to a 1 and the 8 other bits to 0. The switch/ladder/reference network is configured as a digital-to-analog-converter (DAC). The midscale DAC output is compared to the analog bus input. If the input is less than midscale, the MSB is reset to 0 and if the input is greater than midscale, the MSB is retained as a 1. In either case, the next lower bit is then set to a 1 and another comparison performed. Each time the comparison shows the input as less than the DAC output, the current 1 is retained and each time the input is greater than the DAC output, the current bit is reset to 0. The total conversion process takes 22.5 μsec (9 bits at 2.5 μsec each) and is therefore completed at 40 μsec after the beginning of the word boundary. 2.5 μsec after the next word boundary, the contents of the storage register are strobed onto the parallel PCM data bus (digital bus) through the data transfer gates, unless the A/D inhibit line is on in which case no transfer is performed since the presence of an A/D inhibit signal means that a digital module is taking priority over the ADC.

ADC's in general cannot give accurate readings of data which is changing at a rate significantly fast relative to the conversion process itself. The ADC being discussed here is no exception, and its lack of a sample-and-hold circuit combined with the successive approximation technique leads to one particularly interesting phenomena associated with rapidly changing data. Suppose that the input is a low voltage at the beginning of the conversion process and that it goes high rapidly during the middle of the conversion process. As the ADC tracks the input by successive approximations, the digital output of the ADC will be for example 000XXXXXX after 3 bits of approximation. If the data at this point exceeds the value corresponding to 000100000, then the next reading will be 0001XXXXX. Now if the input data is moving rapidly upwards, each successive approximation will add another 1 to the string in a futile attempt by the ADC to catch up to the input data. Thus, the final approximation will be 000111111. Notice that the form of this number is 2^n-1 with, in this case, n = 7. If the data had started moving upward at a different time, the result would be of the same form (2^n-1) but with a different n.

Thus, experimenters are warned that if one of their analog channels has an otherwise unexplainable preponderance of values of the form 2^n-1, then it probably means that their analog data is moving at a rate far faster than can be handled by the ADC of the SRT/MF. This has actually happened during a flight, and as it turned out, the 2^n-1 readings were found to always correspond to the leading edge of a fast pulse on the analog input.

By a similar process, trailing edges (rapidly decreasing analog data) of pulses will frequently show outputs of the form 2^n.

The zero adjust and gain adjust shown in Figure 3.4 are always set so that the relationship between input and output is described by the following equations:

$$\text{Output Counts} = 16 + 96 \times \text{Input Voltage}$$

$$\text{Input Voltage} = \frac{\text{Output Counts} - 16}{96}$$

In other words, the zero-volts bias is 16 counts and the gain is 96 counts per volt (note that this is very close to 10mV per count).

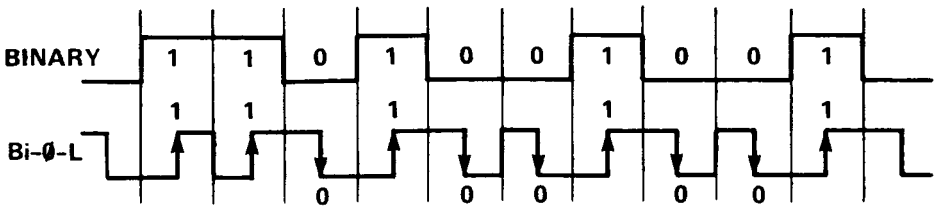
The analog bus (which feeds the ADC) will run throughout the system, physically, and will therefore have a certain amount of stray capacitance. The larger the stack, the larger the stray capacitance. Since the analog input has 17.5μsec during which to change the voltage on this stray capacitance, the input impedance must be low enough that the RC time constant is low relative to 17.5μsec. Without going into the details, suffice it to say that for this reason, the experimenter is advised to keep his analog output impedance below 5K Ohms. Larger impedances will result in "anomalies" of one or more counts on the reconstructed analog data. This topic is discussed further in Section 5.1.

3.5 Output Logic

The output logic section of the SRT/MF is shown in Figure 3.5. It takes in the data on the digital bus (parallel PCM data bus) and puts out 10-bit filtered Bi-Ø-L serial data with odd parity being the 10th bit.

The digital data is loaded into a 9-bit shift register during the data transfer pulse and is shifted out by the 200 kHz bit clock. These signals are shown in Figure 3.0.3. The parallel data is negative-logic and is normally high except during the data transfer pulse at which time a 1 bit will cause its line to go low, resetting the corresponding bit in the shift register. The data is taken out of the shift register on the $\overline{Q}$ output so as to re-invert the data back to positive logic. The shift register serial input is tied to a logical 1 so as to make the shift register end up with all 1's after the data has been shifted out. As can be seen from Figure 3.5, the serial data comes out MSB first, LSB last. As the data goes out, each bit is strobed into a JK flip flop which is wired in the "T" (toggle) configuration. This flip flop is reset before the first bit is shifted out, and then counts the number of 1's in the data. If the number of 1's in the data is odd, the flip flop will end up in a 1 state and if the number of 1's in the data is even, it will end up in the zero state. By taking the $\overline{Q}$ output of the parity flip flop and putting it onto the data stream after the data LSB has shifted out, the total 10-bit data word generated always has odd parity. The parity bit is used by the ground station to identify data transmission errors.

The binary output of this circuit is exclusively-OR'ed with the bit clock so as to produce a Bi-Ø-L output which is then bandwidth-limited by a maximum-linear-phase filter before going to the telemetry transmitter. The Bi-Ø-L signal looks like this:



Note that the Bi-Ø-L signal always has a transition in the middle of the bit-time but it may or may not have a transition at the start of a bit-time. This fact is used by the bit-sync back on the ground to reconstruct the binary waveform. The Bi-Ø-L can be transmitted and reconstructed more reliably and with lower bandwidth than can the binary waveform.

3.6 Power Supply

The power supply section of the SRT/MF is shown in Figure 3.6. It converts the +28 Vdc (nominal) input to the +5V, +12V, -12V and -27V supplies required by the SRT/MF and the various data modules.

Initially, the control module supplies a free-running clock to the synchronous chopper (which means that initially the synchronous chopper is not yet synchronous). When the control logic circuitry (see Section 3.1) begins generating clock signals, the control module of the power supply switches from its internal clock to the 20kHz system clock to cause the power supply synchronous chopper to run synchronously with the system clocks thereby avoiding potential noise problems which might occur if the chopper were to run asynchronously. This process will automatically reverse if the system clock fails. The 20kHz clock (synchronous or internal) is divided by 2 and both polarities are fed to the chopper.

The hybrid regulator senses only the +5 Vdc line and the other outputs are slaved to the +5 V line. Transient protection on the input is provided by the suppresor diode CR1. Bridge rectifiers and capacitive filters are used on each output. Internal current-limiting allows the power supply to sustain a short circuit for 30 seconds without permanent damage.

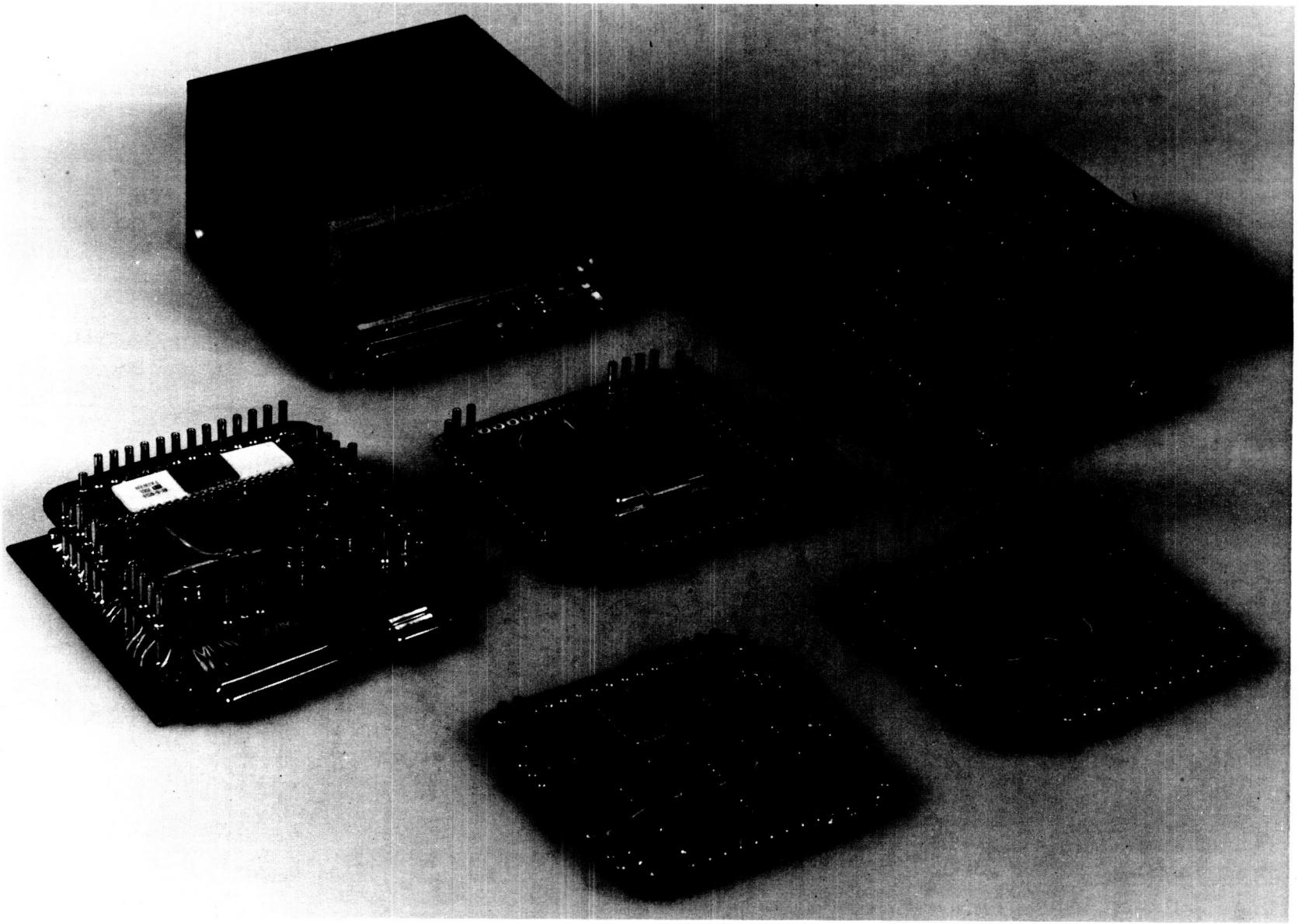


Figure 3.0.1. SRT/MF (Several Views)

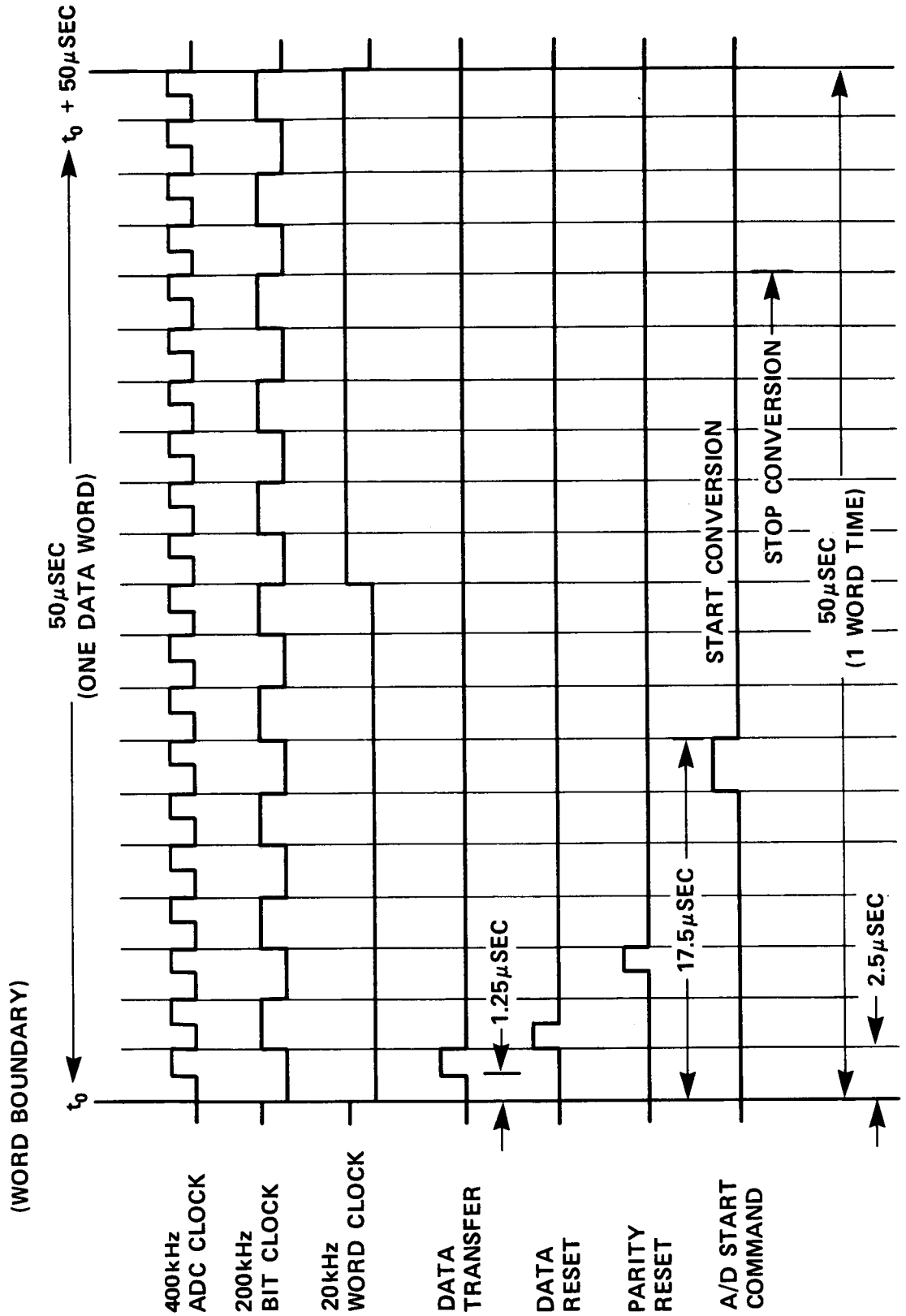


Figure 3.0.3. SRT/MF Timing Diagram

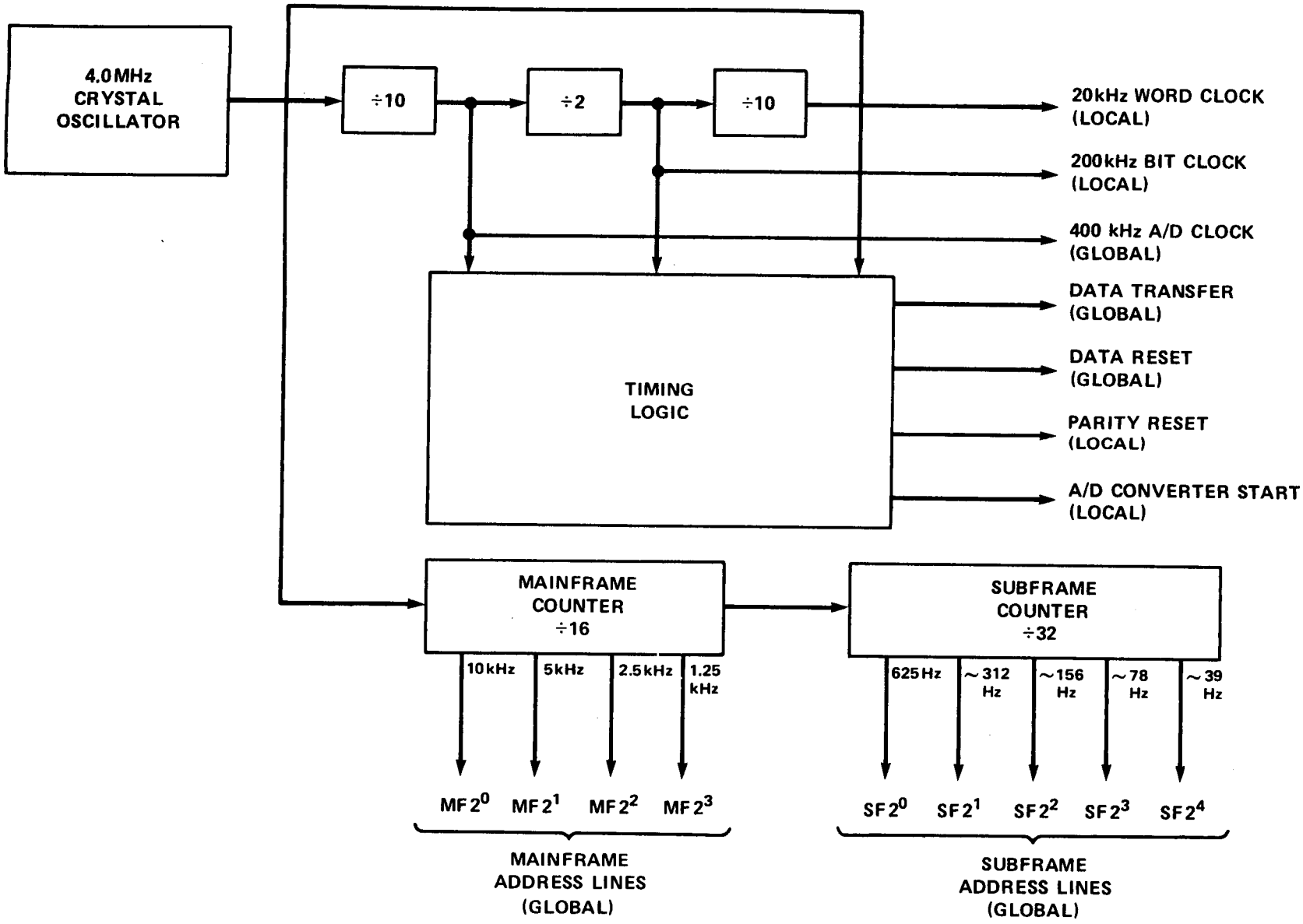


Figure 3.1. Control Logic Block Diagram

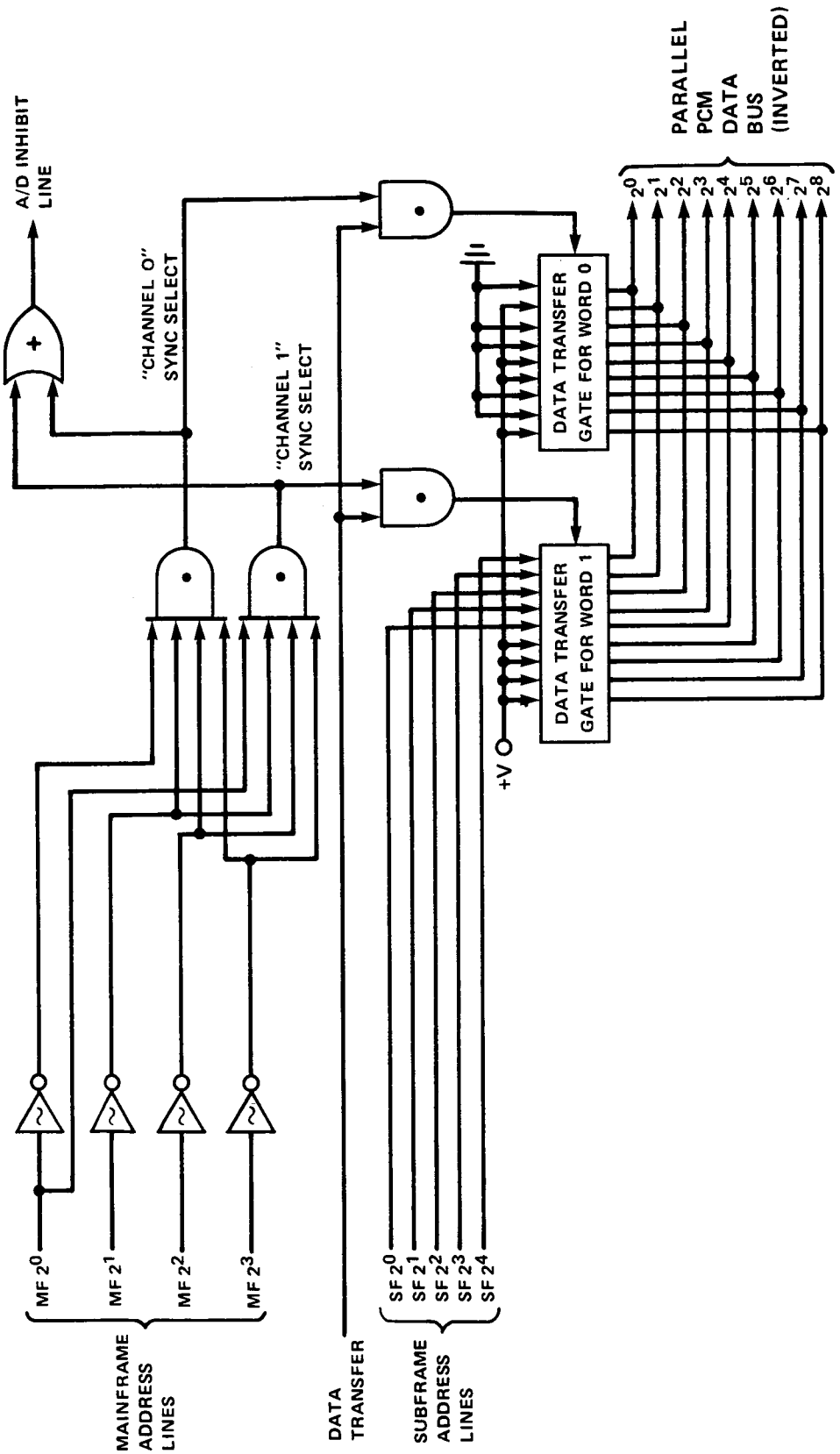


Figure 3.2. Sync Code Generator Block Diagram

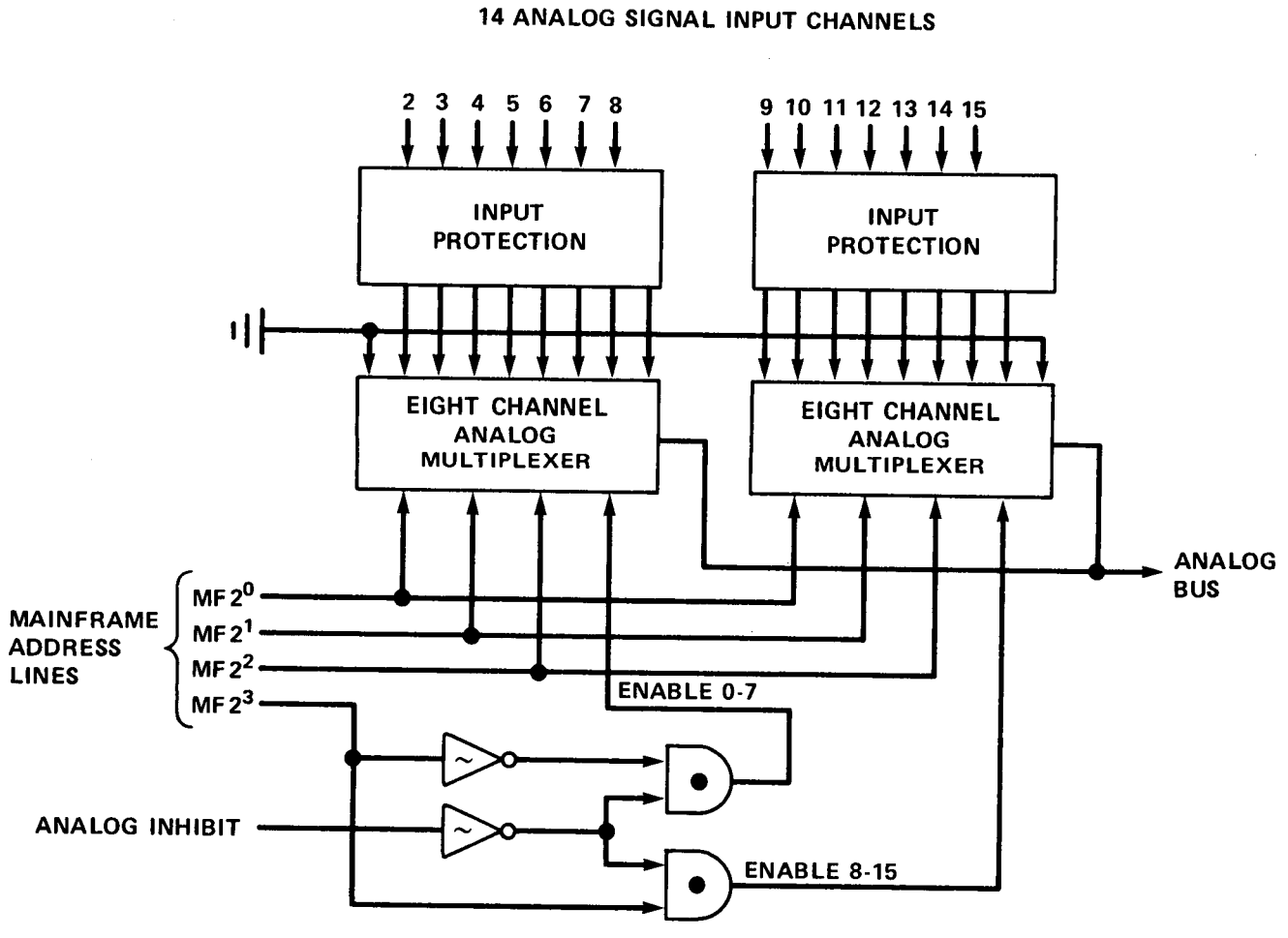


Figure 3.3. Analog Multiplexer Block Diagram

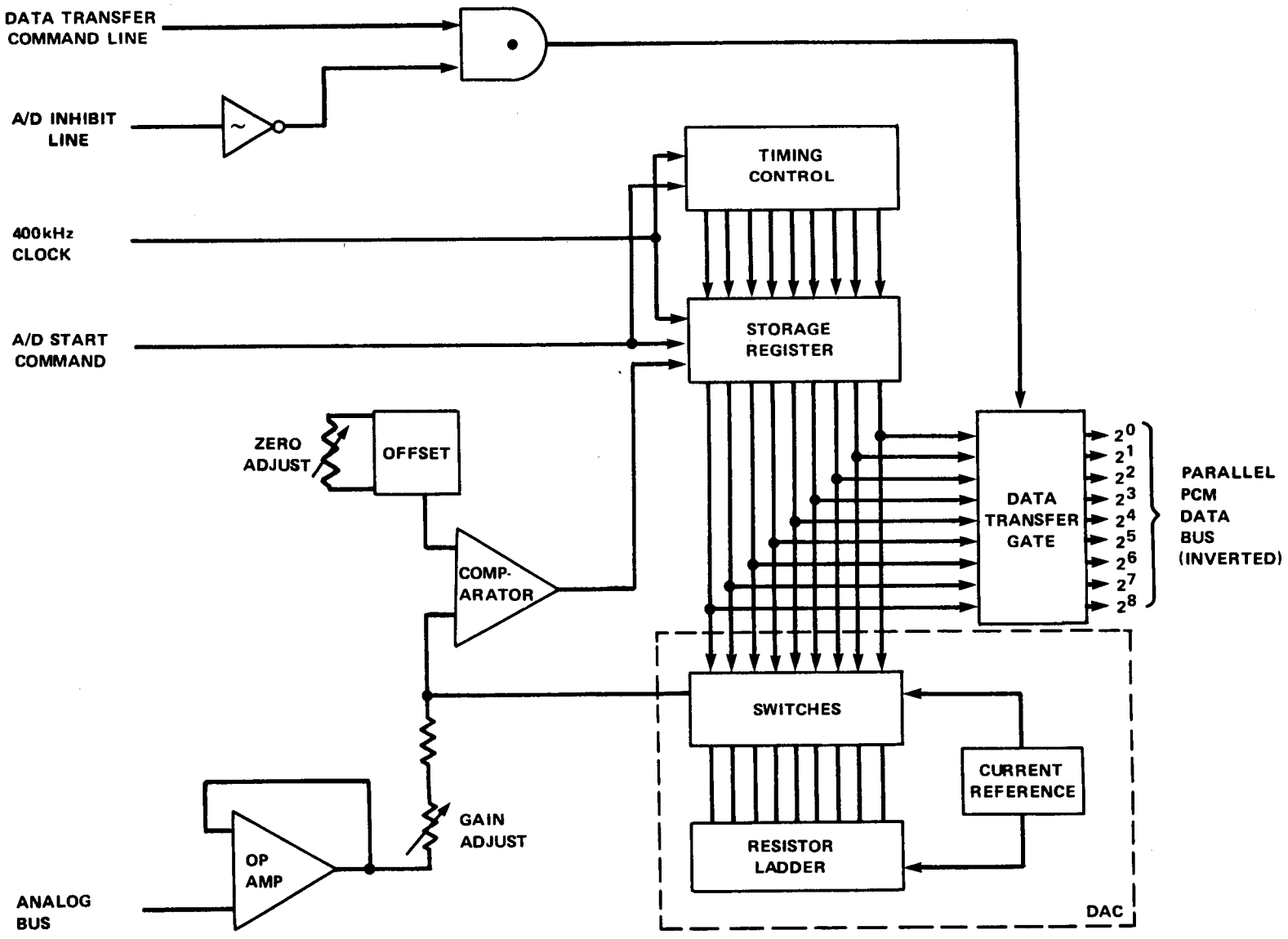


Figure 3.4. Analog-to-Digital Converter Block Diagram

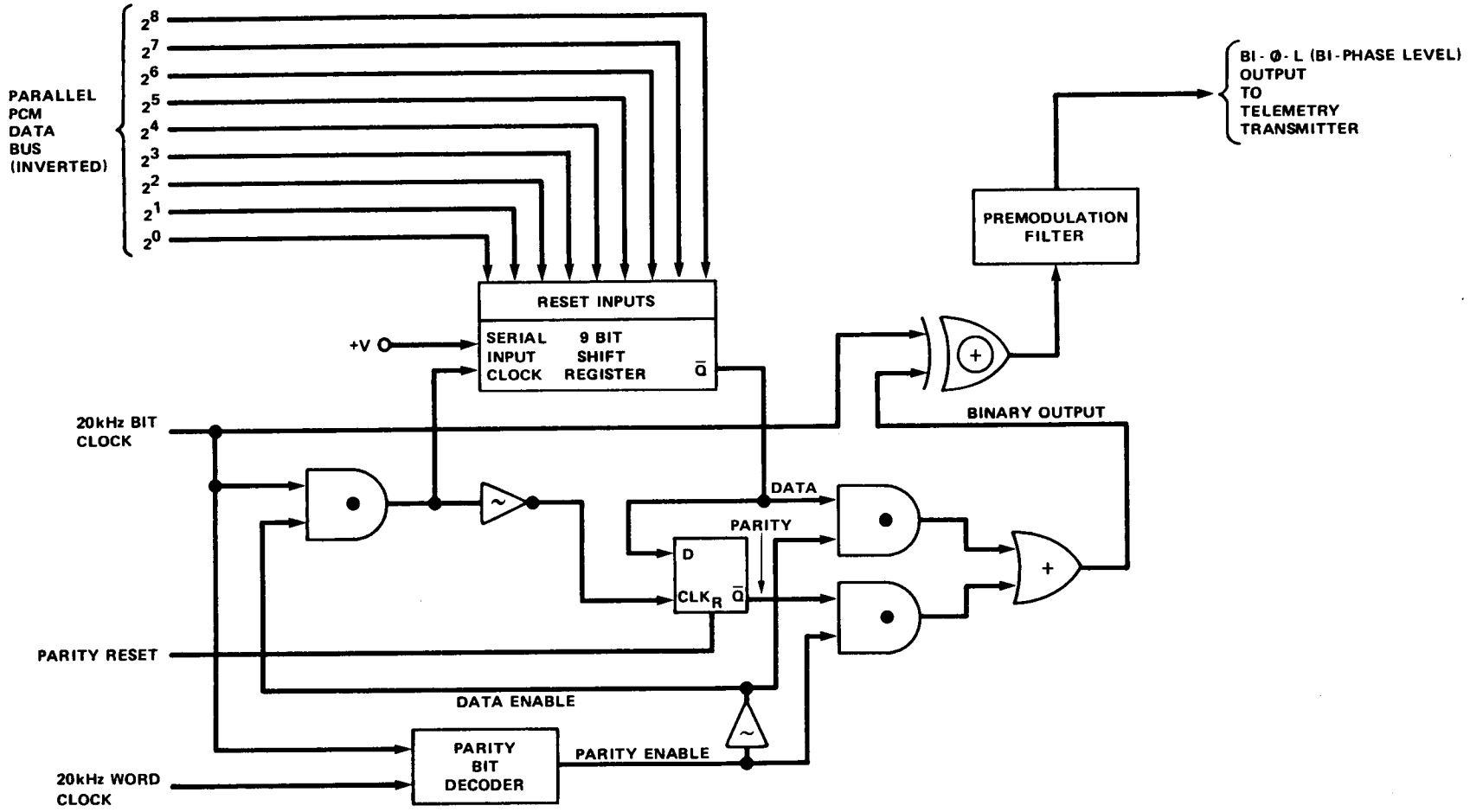


Figure 3.5. Output Logic Block Diagram

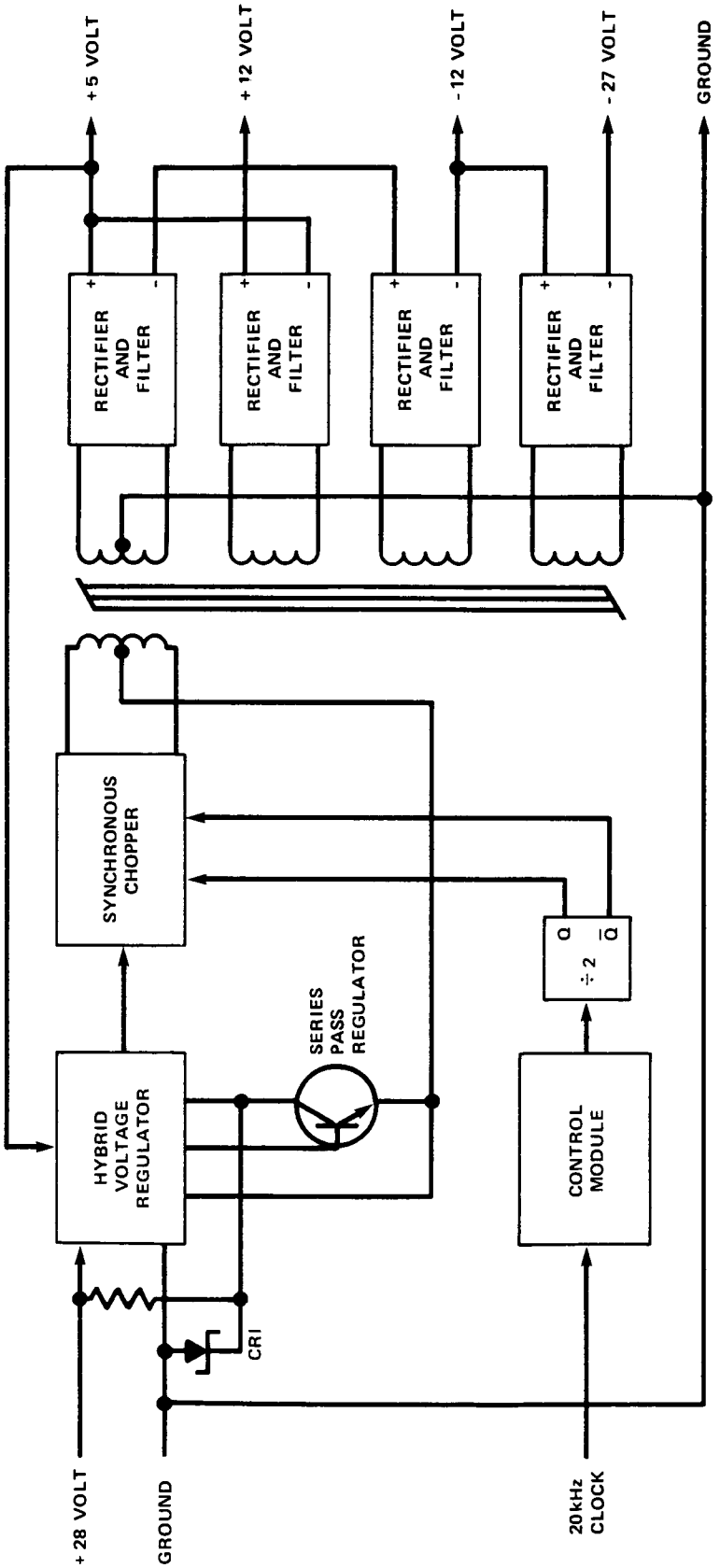


Figure 3.6. Power Supply Block Diagram

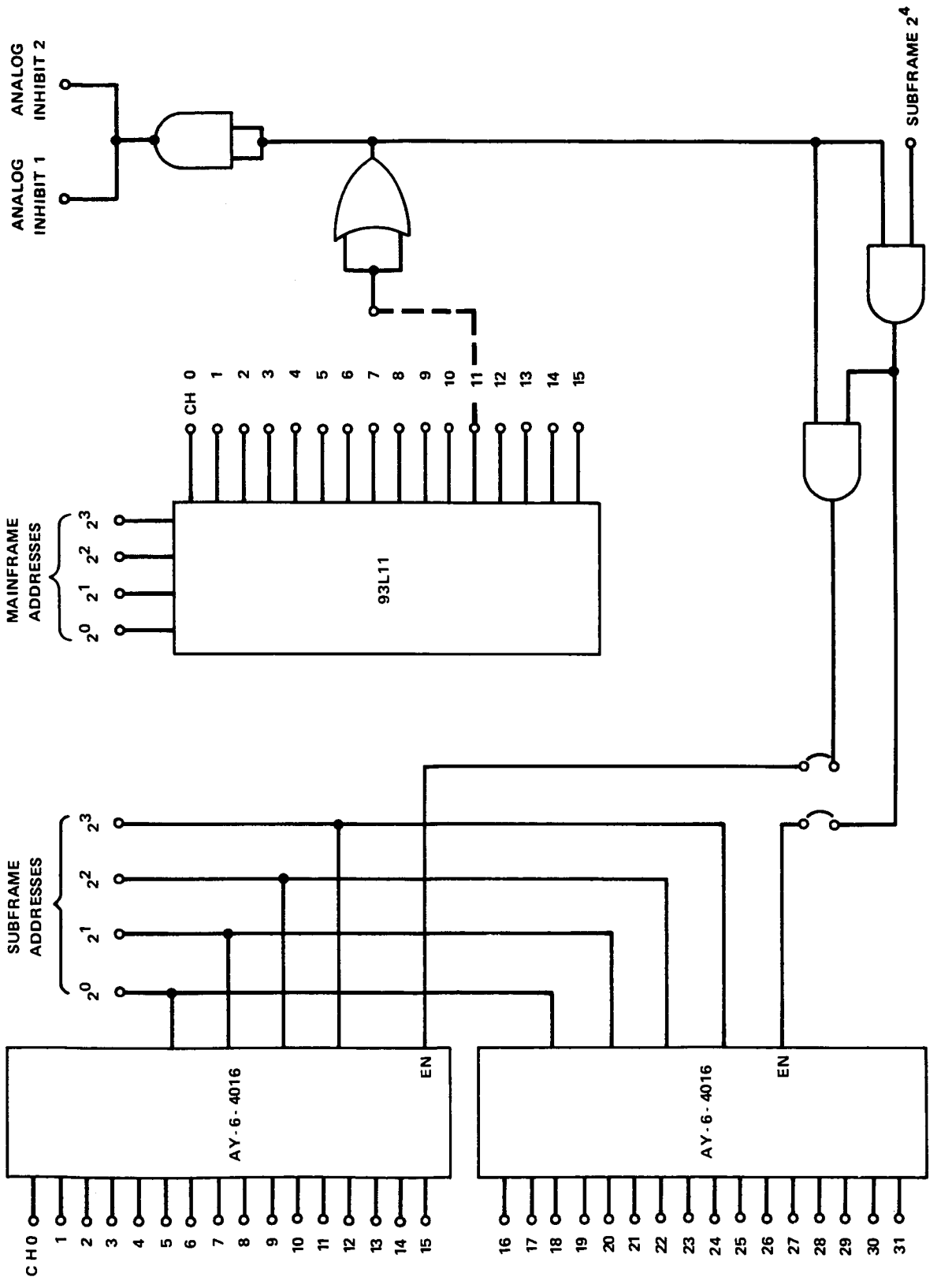


Figure 3.7. PAD Block Diagram (Analog)

4.0 Expansion Techniques

The expansion techniques used in this data collection system are based on the general concepts of priority and bus structures as used by most minicomputer and microcomputer systems. The data modules are examined in much the same way as peripherals are examined by a computer. Additional flexibility is provided by use of a programmable ROM to handle "device addresses" (i.e. data module addresses) which may be arbitrarily assigned according to the hard-wire programming of modules currently stocked by Code 743.4. The ROM converts the arbitrary module addresses to the data-matrix addresses desired by the experimenter.

The 14 mainframe channels of the data matrix (Figure 2.0.2) can be expanded to as many as 32 data channels each for a total system capability of 448 (=14 x 32) data channels. These can be any combination of analog, digital, etc.

NOTE: The system prior to 1974 had a limit of 16 subchannels per channel for digital modules. This limitation no longer exists and experimenters who have not used the system since 1974 are cautioned to re-examine their data-matrix assignments in light of this new flexibility.

4.1 Priority

The priority of the system data collection is hardwired as follows:

Highest Priority: Digital Data Modules (i.e. all modules except for the AS-32 and the ASC-32)

Middle Priority: Analog Data Modules (the AS-32 and the ASC-32)

Lowest Priority: SRT/MF analog inputs (the 14 mainframe channels)

The priority is accomplished by the use of two control signals as shown in Figure 2.0.3. The analog inhibit line allows analog modules to over-ride the SRT/MF inputs and the A/D inhibit line allows digital modules to over-ride all analog data by disabling the A/D converter output. Figure 2.0.3 is, of course, a logical representation only – the actual circuitry does not use mechanical switches.

4.2 Programmable Address Decoder

The SRT/MF puts out a 9-bit address (see Section 3.1) which consists of a 4-bit mainframe address and a 5-bit subframe address, which produces the 16 x 32 word data matrix ($16 = 2^4$ mainframes, $32 = 2^5$ subframes). The address decoder for the SRT/MF analog inputs is shown in Figure 3.3. The address decoder for the AS-32 and ASC-32 is shown in Figure 3.7. All modules other than the analog modules have a programmable address decoder as shown in Figure 4.2.

> NOTE: Readers not familiar with the "C-S-D" assignment code should read chapter 8 of this report before proceeding with the current section.

Although the decoders allow a module to have an address of anything from C-S-Ø to C-S-4, the modules as purchased are always programmed to be C-S-4, and the PAC-16 (see Section 4.3) is used to provide the address actually desired by the experimenter. Because of the limit that the programmable address decoder can only go to C-S-4 and not C-S-5, there cannot be more than 16 subframes per channel-address. This most emphatically does NOT mean, however, that the

data matrix itself is limited to 16 subframes per channel. The PAC-16 can be used to give up to 32 subframes per channel for digital data. This will be explained more fully, with examples, in Section 4.4. The one limitation on the system which is imposed by the inability of the modules to be directly addressed as C-S-5 is that the total number of inputs which can be addressed by the system is only 16 x 16 = 256. As will be further explained in Section 4.4, the actual total is 256 + 32 = 286 data inputs. For simplicity, the number 256 ($=2^8$) is generally used.

4.3 Programmable Address Converter (PAC-16)

The PAC-16 is shown in block diagram form in Figure 4.3.3; photos are shown in Figures 4.3.1 and 4.3.2. It consists primarily of a pair of Intel 1702A EPROM's which are 2048 bits each organized as a 256-bit by 8-bit array. The 1702A is erasable by application of ultraviolet light. Programming is accomplished by using any of several different types of ROM-programmers available in the SRD.

The 9-bit PCM address lines are input to the PAC-16. The input bit SF 2^4 (MSB of the subframe count) is used to select one of the two PROMS and the remaining 8 address lines are used to address the PROMS which are programmed such that each input address is converted to an output address (the PROM output data is looked at as the PCM address by everything stacked above the PROM).

The PAC-16 acts like a look-up table to convert any 9-bit address to any other arbitrary address (but only of 8 bits). Thus, the programmable address decoders (see Section 4.2) of each data module need only be programmed for a unique mainframe address ($0 \rightarrow 15$) and subframe address ($0 \rightarrow 15$, not $0 \rightarrow 31$) and the PAC can construct any data format desired.

Just as an example, consider in Figure 8.0.3 the entry C1. This entry is designated 5-0-3; it appears in channel 5, subframes 0, 8, 16 and 24. The counter module assigned to this input might have, for example, the designation 6-12, 13, 14, 15-4 (this is the designation of the 4 address decoders on the module). Suppose further that circuit #2 (address 6-13-4) is the one assigned to the input which we desire to come out on 5-0-3. The PAC-16 ROM's would then be programmed so that input address 4-0, 4-8, 4-16 and 4-24 all* put out the 8-bit address 6-13. In this way the PAC selects the desired circuit of the appropriate module so that a given input is placed into the data matrix at the appropriate time. All programming of the PAC is determined in a similar fashion, and the data matrix is thereby constructed to the experimenter's specifications without any need to rewire the address decoders in the data modules. The technique is clearly amenable to quick changes should the data format requirements change.

The output of the PAC-16 is the 8-bit address (lacking the SF 2^4) plus the 10kHz clock which is used to drive the booster power supply (see Section 6.0) if one is used. The 10kHz clock is put on the line which is SF 2^4 below the PAC. Above the PAC the SF 2^4 is not required since it is not used by the address decoders.

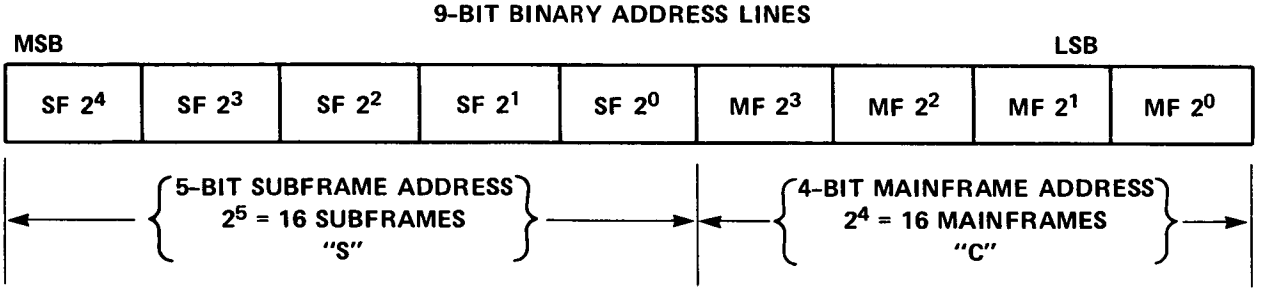
4.4 Addressing Techniques

The programmable address decoder (see Section 4.2) and the programmable address converter (PAC-16, see Section 4.3) combine with the PCM address lines (see Section 3.1) to form a highly

*NOTE: The use of channel 4 (rather than 5) is not a typographical error. Details in Section 4.4.

flexible addressing scheme. This flexibility leads to at least a minor amount of complexity and there has been some confusion on the part of system users as to exactly how the overall addressing scheme works. The purpose of this section is to explain, and give examples of, the ways in which the addressing scheme works.

First, let us consider the basic PCM address lines generated by the control logic of the SRT/MF (see Section 3.1). The address consists of 9 lines; 4 frame-address lines and 5 subframe-address lines. This gives a total of $2^4 = 16$ by $2^5 = 32$ data addresses, as shown in the data matrix of Figure 2.0.2. These address lines are binary-sequential. That is, they progress from a count of binary 000000000 to a count of binary 111111111, with the most significant binary bit being subframe address 2^4, and the least significant being mainframe address 2^0. The address lines, then, have the following logical structure:



If this is your first reading of the book, a reading of Chapter 8 is recommended prior to continuation of this Section.

The subframe address is the "S" of the C-S-D code discussed in Chapter 8, and the mainframe address is the "C" of the C-S-D code. Thus, the 9-bit binary sequential address lines start at a C-S-D code of 0-0-5 and end at 15-31-5, with the data matrix address progressing from left to right within a row and then back to the left of the next row down. The time per word is 50μsec and thus the time from 8-3-5 to 9-3-5 is 50μsec but the time from 8-3-5 to 8-4-5 is 800μsec since the count goes 8-3, 9-3, 10-3, . . . , 15-3, 0-4, 1-4, . . . , 7-4, 8-4 for a total of 16 words (x50μsec = 800μsec) between 8-3-5 and 8-4-5.

All of this discussion about the relationship between time (in 50μsec intervals) and the data address may seem tediously obvious; the relationship is discussed so fully because it will be pointed out later in this section that above the PAC-16, the "obvious" time relationship just discussed does not hold at all, and it will prove useful for the reader to be absolutely clear what the relationship is that "does not hold" above the PAC-16.

The programmable address decoders, as discussed in Section 4.2, provide a means whereby jumper wires may be used to assign data to particular matrix formats. These programmable address decoders were part of the original system design and are now considered too inflexible for the desired system characteristics. They also have the disadvantage of requiring resoldering of jumper wires to reprogram a matrix. Thus the PAC-16, which will be discussed shortly, was developed. The programmable address decoders are now ordered pre-wired by the manufacturer in various configurations and reprogramming is no longer accomplished by changing jumpers.

Before any further discussion of the programmable address decoders the PAC-16 will now be discussed. As was stated in the previous paragraph, the PAC-16 was developed to overcome limitations

in the flexibility of the programmable address decoder. When the system was first designed, the EPROM's used by the PAC-16 were experimental and not widely available, so the lack of a PAC-16 was not an oversight in the original design, it simply was not economically feasible at the time.

The PAC-16 is, very simply, a look-up table using EPROM's for flexibility in reprogramming. The 9-bit PCM address is used as an input to the EPROM look-up table, and what comes out of the EPROM then becomes the PCM address for all modules physically located above the PAC-16 in the PCM data-module stack. For several reasons – the most significant being the 8-bit organization of the EPROM's – the PCM address above the PAC-16 is only 8 bits, the "lost" bit being the SF 2^4 bit. Because 2 EPROM's are used (see Figure 4.3.2) in the PAC-16, a total of 256 + 256 = 512 different inputs can be used. That is to say, the "lost" SF 2^4 output is not thrown away at the input but rather is used to select one of two EPROM's. Thus, every one of the 512 data matrix positions (i.e. every one of the 512 states of the PCM address lines) corresponds to an entry in the look-up table. The output of the look-up table, however, is only 8 bits and therefore can select only 2^8 = 256 different data values. This means that although the data matrix contains 512 entries, 448 of which are reserved for data, those modules above the PAC-16 can contribute only 256 distinct data values towards filling the matrix. As a result, if there are no data modules below the PAC-16, then the 448-position data matrix will be filled by, at most, 256 distinct data sources. This is not a limitation in any practical sense, since only one experimenter in 6 years has required more than 160 data sources, and the vast majority of experimenters use under 120 data sources; this includes, typically, 20 housekeeping functions required by the Payload Design Section, the Payload Operations Section and the Analysis Section, as well as another 20 sometimes required by the Attitude, Control and Stabilization Branch.

Also it is entirely feasible to have some modules below the PAC-16 and any such modules do not reduce at all the 256 data points available as inputs to the data modules above the PAC-16. In fact, PCM stacks are arranged 9 times out of 10 such that at least one module, the ASC-32, is below the PAC-16. The primary reason for this is that all rockets have a certain minimum of analog housekeeping data (battery monitors, etc.) and it was decided that an ASC-32 below the PAC-16 was ideally suited to this function. This ASC-32 below the PAC gives 30 channels of analog data and thus the total number of channels available is the 30 below the PAC-16 plus 256 above the PAC-16, for a total of 286. The rare case where a stack does not have an ASC-32 below the PAC-16 is the second PCM system on flights which have two full PCM systems. These second systems, when used, are invariably dedicated to a very small number of data inputs (frequently just one) which are sampled at a very high rate.

The programmable address decoders are combinatorial logic (see Figure 4.2) and therefore decode the 8-bit address lines in real time. As was discussed in Section 3.0, the conversion time for analog data and the accumulation time for serial input to the SIDL-16 both require a 50μsec set-up time, requiring data which is to be output at channel C-S-D to be addressed at channel (C-1)-S-D. With no PAC-16 this is straight-forward and is accomplished by programming the PAD for C-1 rather than C. With the introduction of the PAC-16, however, things become slightly more complicated as illustrated by the following example: - Suppose that a SIDL-16, for example, is purchased with its PAD hardwired for 10-0, 1, . . . , 14, 15-4, and further suppose that the experimenter desires the data on the first SIDL-16 circuit (PAD wired for 10-0-4) to be assigned to the matrix position 8-3-3. Without the PAC-16, the 8-3-3 assignment could be accomplished only by rewiring the SIDL-16's PAD for 7-0, 1, . . . , 7-3 which would cause half of the SIDL-16's data inputs to be wired out of existance. Channel 7 was chosen so that the data would come out during channel 8 as the experimenter desired. With the PAC-16, however, it is not necessary to rewire the SIDL-16's PAD, nor is it necessary to eliminate half of the SIDL-16's data channels. In the example chosen, the solution is to have the look-up table output the address 10-0 when the PAC-16 input is at 7-3-3. The important consideration here is the time relationship between PAC-16 input and addresses into PAD's. The relationship is such that the address into the PAD

can be whatever one desires it to be (an arbitrary 10–0 in the current example) but it must be issued at (C–1)–S–D where the output data is desired at C–S–D. The binary sequential time relationship of the address lines clearly does not hold above the PAC–16. The address lines above the PAC–16 are purely random although once assigned for a given matrix configuration they do not vary unless the EPROM's are reprogrammed.

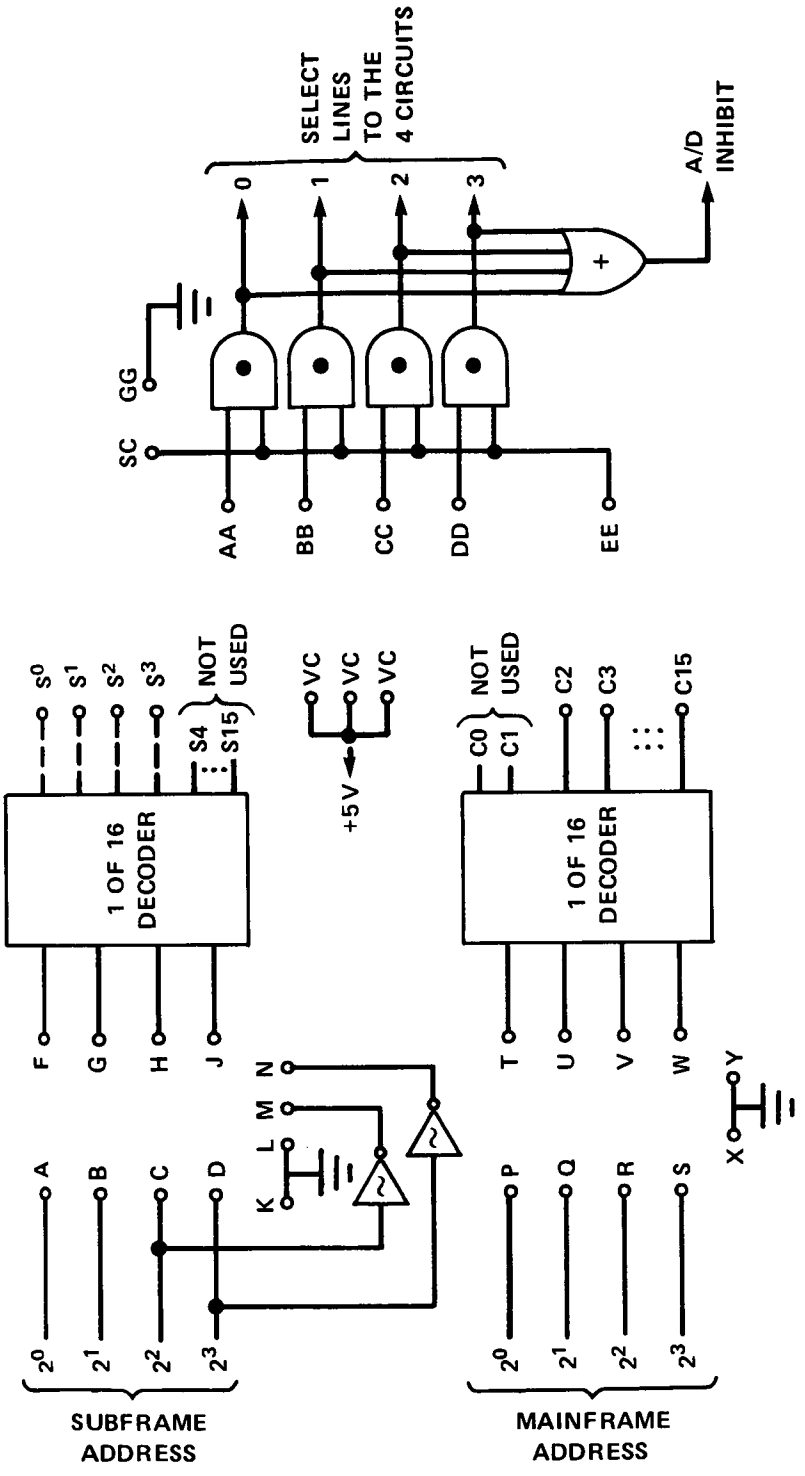


Figure 4.2. PAD Block Diagram (Digital)

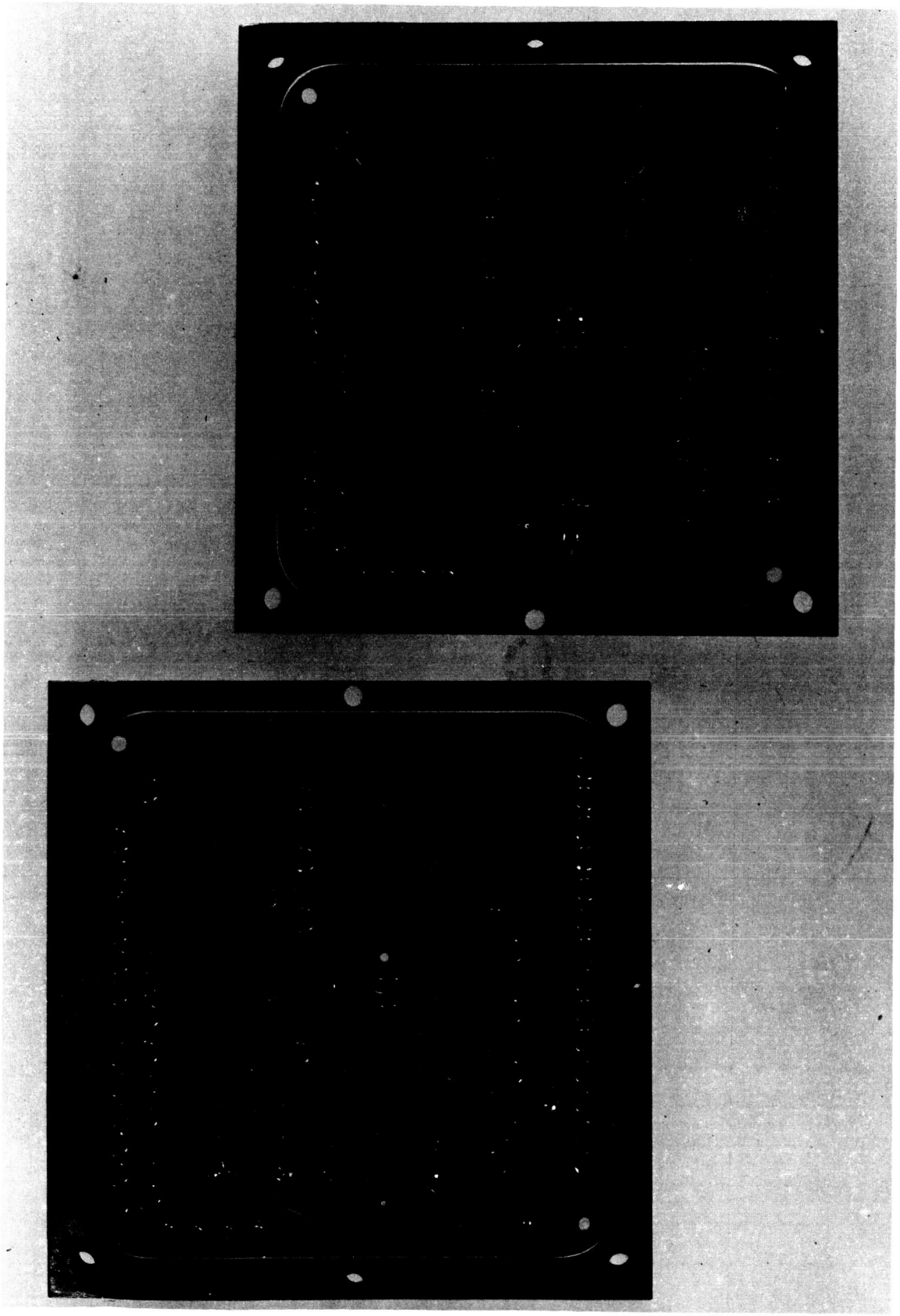


Figure 4.3.1. PAC–16

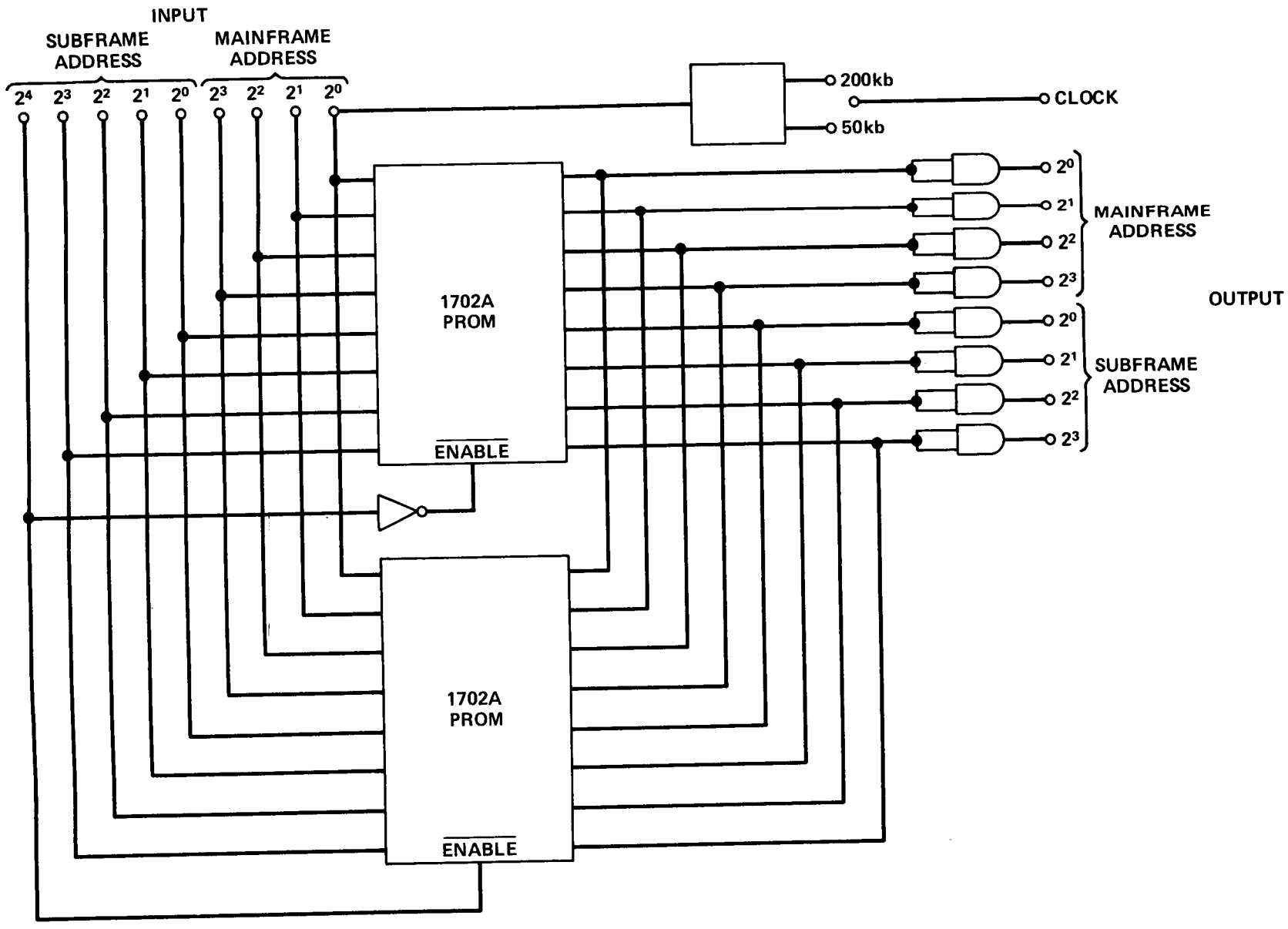


Figure 4.3.2. PAC-16 Block Diagram

5.0 Data Modules

The data modules available for use with the system are as of this writing:

AS-32 32-Channel Analog Multiplexer

ASC-32 Same as AS-32, but with 30 analog channels, one 9-bit parallel digital input, plus an internal analog calibrator.

RCM-4 4-Channel Count-Rate Accumulator

SIDL-8 4-Channel Serial Digital Data Loader

SIDL-16 16-Channel Serial Digital Data Loader

BUF-4 Signal Buffer

TEM-4 Time Event Monitor

RBM-4 4-Channel, 9-bit (per channel) parallel digital data loader.

BPS-5 Booster Power Supply (for use with large stacks).

PAC-16 Programmable Address Converter

These modules all plug directly into the SRT/MF and/or into each other. The only limit as to how many modules can be stacked is a power-supply limit, the details of which are discussed in Section 7.0. When the power-supply limit has been reached, a "Booster Stack" starting off with a Booster Power Supply (BPS-5) can be used for additional modules.

As was discussed in Section 4.2, each data module has an address decoder which allows any of its data inputs to be programmed by the PAC-16 into any position of the data matrix. Physical specifications for each module are given in Appendix A.

A summary of interfacing specifications is given in Appendix B. The pin assignments for each module are given in Appendix C. In general, the experimenter need be concerned only with Appendix B, since pin assignments, channel assignments, etc., are organized by Code 743.4.

5.1 Analog Submultiplexer (AS-32)

The AS-32, shown in Figures 5.1.1 and 5.1.2 has 32 analog inputs which it can multiplex onto the analog bus. Each analog input is protected with a diode clamp circuit to provide both reverse and overvoltage protection up to ±35Vdc. The AS-32 consists of two 16-channel MOS multiplexers that are controlled by an external address decoder as well as their own 4-bit address decoders. The outputs of the mux's are buffered onto the analog bus so that there is minimal capacitive loading on the analog bus. Earlier versions of the AS-32 did not have this buffering and, in an experiment requiring 10 AS-32's in one stack it was found that the capacitive buildup on the analog bus was too great to maintain 9-bit accuracy so the buffer was added.

As can be seen in Figure 5.1.2, the on-board mainframe decoder selects one of the 16 mainframe addresses as part of the AS-32 address decoding. If the AS-32 is being used without a PAC-16

module then the address selection is similar to that explained in Section 3.3. The selected address is one less than the number of the channel during which it is desired that the data appear in the PCM data stream.

In actual practice, a PAC-16 would almost always be used, and would be programmed such that the address of a given submodule (which is hard-wire programmed) could be outputted with the input of an arbitrary address. This would allow very flexible location and sampling rate of various data in the data matrix.

As an example, consider one piece of data fed into an AS-32 which is hardwire programmed for channel 12-0-4, 12-1-4, etc. Without a PAC-16, the data would appear in channel 12-0 and 12-16 with a sample rate of approximately 79 samples per second. Using a PAC-16, this one piece of data could theoretically appear in each one of the 448 available spaces in the matrix and be sampled at a rate of 39 x 448, or 17,472 samples per second.

5.2 Analog Submultiplexer with Calibration and Bi-Level Monitor (ASC-32)

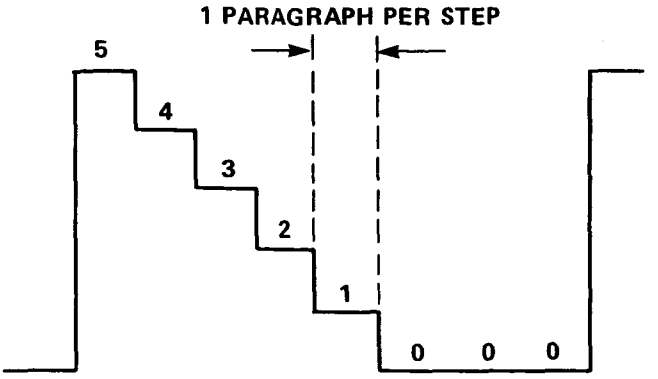
The ASC-32 is an AS-32 plus a second board which provides a precision analog voltage calibrator and also nine 1-bit bi-level event monitors. The top board, shown in Figure 5.2.1 is only slightly different from the AS-32 (Figure 5.1.1). As can be seen from Figure 5.2.3, the only significant difference between an AS-32 and the top board of the ASC-32 is that the ASC-32 uses subframe 31 for the calibrator voltage from the bottom board, and the subframe 0 analog input is not connected at all since the bottom board uses subframe 0 for the bi-level monitors.

The calibrator (see Figure 5.2.3) on the bottom board consists of a zener voltage reference supply and amplifier, a precision resistor divider network, an eight-channel multiplexer, a modulo-8 counter and a buffer amplifier. The bi-level monitor function consists of a "subframe 0" detector and a 9-bit data input protection circuit followed by a 9-bit transfer gate. The five subframe address lines are first buffered and then AND'ed together with the logic signal that determines the mainframe channel in which the bi-level monitor information is to appear. The output of the AND gate will be true only in subframe 0. The output of this AND is also used to inhibit operation of the A/D converter in the SRT/MF via the A/D inhibit line.

The enabling logic level for the data transfer gates is the AND of the subframe 0 detector and the data transfer signal from the main encoder. The 9-bit data is then strobed onto the parallel PCM data bus at the proper time in subframe 0.

Although the bi-level monitors of the ASC-32 were designed expressly for bi-level functions such as "door open", "switch closed", etc., they do represent a 9-bit parallel digital input and can be used as such rather than as nine separate 1-bit monitors.

The calibrator reference voltage is obtained from a zener supply that is the input to a fully compensated inverting amplifier with a gain of less than one. The +5.0Vdc reference output of the amplifier is divided down into +4.0, +3.0, +2.0 and +1.0 volt levels by a precision resistor network. The five reference voltages, along with a reference ground, are then multiplexed into subframe 31 of the selected mainframe channel. The divide-by-eight counter which steps the multiplexer is driven from the MSB of the subframe address; the sequence of reference voltages is: +5V, +4V, +3V, +2V, +1V, +0V, +0V, +0V as seen below.



ANALOG CALIBRATOR WAVEFORM

There is no particular significance to the calibrator sequence; it was an arbitrary choice based on ease of implementation. The reference voltages are buffered by a non-inverting amplifier in a follower configuration and then sent to the top board to be multiplexed onto subframe 31 of the ASC-32 channel. The buffer amplifier has a zero volt adjustment for precise control of the calibration voltages.

Because the ASC-32 contains the in-flight calibrator for the ADC of the SRT/MF, the ASC-32 is always the first analog module assigned to any stack. If additional analog inputs are required on a flight (as they usually are) AS-32's are assigned as necessary. Most rockets require at least some very low frequency "housekeeping" data such as battery monitors, etc., so assignment of the ASC-32's analog data to a 40 sample per second rate seemed appropriate, and channel 15 was chosen for the ASC-32's. The ASC-32 has to be below the PAC-16 (if one is used) because the calibrator sequence is derived from the SF 2^4 signal which is not present above the PAC-16. Once the decision was made to always put the ASC-32 on channel 15, the ground station equipment was designed to use the in-flight calibrator assuming it to always be in 15-31-5. Thus:

> Experimenter's Note: The ASC-32, if used, will always be programmed for channel 15.

Hindsight shows that channel 8 or 9 would have been a better choice because of the conflicts which using channel 15 causes when several signals need to be evenly supercommutated onto several mainframe channels. However, this is a relatively rare annoyance and it is not felt that the minor advantage to be gained would justify the major effort required to both reprogram all ASC-32's and also modify the ground stations to accommodate a channel 8 or 9 calibrator.

5.3 Counter Module (RCM-4)

The RCM-4 shown in Figure 5.3.1 accumulates input pulses in four independent counter channels and, upon command, transfers the accumulated counts to the parallel PCM data bus (digital bus). The RCM-4, as diagrammed in Figure 5.3.2, consists of four independent 9-bit binary counters each with its own set of data transfer gates connected to the digital data bus, and a programmable address decoder that controls the input gating and data transferring operations for each of the counters. At one time there was an optional jumper for allowing each counter to be reset after it was sampled. Experimenters accustomed to using the reset feature please note:

> THESE COUNTERS CANNOT BE RESET!

Each 9-bit counter is preceded by an inhibit gate which disables the input pulse during the one-half bit-period at the beginning of the mainframe channel boundary during which the data is transferred to the parallel PCM data bus. This allows the last input count plenty of time to ripple through the counter (if necessary) and thus assures that the counter will have a stable value while it is being read out. If an input pulse is received during the inhibit, it will be captured in the one-bit memory of the inhibit logic and then automatically entered into the counter immediately following this period. If a second pulse should occur, also during the inhibit period, it will reset the one-bit memory and thus not only be lost itself but also cause the first pulse to be lost. This is not a severe limitation since a pair of pulses during the inhibit time would imply a burst rate of about 500kHz into the counter, and while these counters will perform at that rate, it is very rare for them to be used at so high a frequency.

Each counter overflows after 511 input pulses, and continues counting up from zero again. During the mainframe channel readout period for each counter, the A/D converter in the SRT/MF is disabled by the A/D inhibit line (see Figure 2.0.1 and 2.0.3) which is signaled by the PAD of the RCM-4.

The MSB output of each counter is brought out of the RCM-4 connector (see Figure C.9) and may be used as the input to another counter. This technique allows an 18-bit counter (or even a 27-bit counter) to be formed. Since the two 9-bit counters making up such an 18-bit counter are sampled at different times, however, it is possible for incorrect readings to occur if overflow of the least significant 9 bits occurs between the time of sampling the two counters. This is a minor anomaly and can be easily removed during computerized data reduction by the experimenter.

5.4.0 Serial Input Data Loader (SIDL)

5.4.1 Serial Input Data Loader Module (SIDL-8)

The SIDL-8 accepts nine bit serial input data words into four independent register channels and upon command, transfers the data to the parallel PCM data bus. The SIDL-8 consists of four independent serial to parallel data conversion registers, each with its own set of data transfer gates, and a programmable address decoder that controls the input data gating and data transferring operations for each of the registers. The module also provides an external channel gate signal for each register channel and a data shift clock.

The channel gate signal is used to enable an external serial data source for shifting its information into the selected nine bit register with the 200kHz data shift clock that is provided. The selected nine bit serial word is shifted into the register during the mainframe channel preceding its actual location in the PCM format. Each of the nine bit serial data registers are designed so that they are able to accept input data on a continuous basis. If serial data is being supplied on a continuous basis, only the nine bits of data bracketed by the selected channel gate signal will be transferred to the parallel PCM data bus. (The detailed timing relationships between the gate signal and the data shift clock are given in Appendix B.)

The four registers are not reset after the data has been transferred since the new serial information will automatically replace any old data contained in the registers. The reset command from the encoder is used, however, in order to provide a delayed address gate signal. The delayed address gate and the data transfer command enable the data transfer gates so that the register information is loaded into the encoder format in proper sequence. The A/D converter in the encoder is disabled at the proper time by the delayed channel gate from each register which forms the A/D inhibit line.

5.4.2 Serial Input Data Loader Module (SIDL-16)

The SIDL-16 accepts sixteen 9-bit serial words into a time-shared register which transfers the data to the parallel data bus in the mainframe unit. The programmable address decoder provides for data gating and transfer. In addition to a channel enable output for each of the sixteen inputs, other outputs available are a 200kHz clock, a gated 200kHz clock, and a 5μsec gate. (See Figure 5.4.2.3.) General operation is otherwise as discussed in the paragraph outlining the SIDL-8 operations.

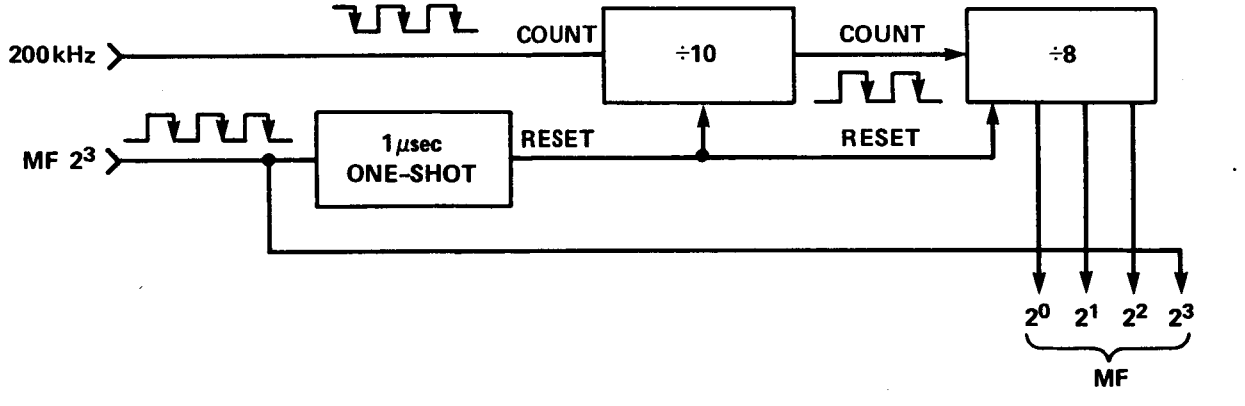
5.5 Signal Buffer (BUF-4)

The BUF-4 shown in Figure 5.5.1 provides the experimenter with access to a number of internal encoder timing signals as shown in Figures 5.5.2 and 5.5.3. These signals can be used for synchronization, timing, multiplexing and whatever else the experimenter desires. The most commonly used signals are provided in both polarities. Each signal is double-buffered so that the operation of the encoder will not be jeopardized by an accidental short or overvoltage on any of the BUF-4 outputs. Two auxiliary inverters are also provided for use by the experimenter. These circuits can be used for example to give the opposite polarity of those signals provided by the buffer in only one polarity.

As is shown in Figure 3.1, the 200kHz clock is local to the SRT/MF. This signal is re-generated on the BUF-4 in the same way as on the SIDL-8 (Figure 5.4.1.2) and the SIDL-16 (Figure 5.4.2.2) and is then provided to the experimenter in both polarities.

Since the address lines out of the BUF-4 are intended to be the SRT/MF address lines, it is necessary that the BUF-4 be placed physically below the PAC-16 when there is a PAC-16 in the stack. If the BUF-4 were placed above the PAC-16, the address lines out of the BUF-4 would be the converted signals, and thus useless for most applications.

Although the low-order 3 bits of the mainframe address lines are not brought out of the BUF-4, they can be generated rather easily, if required, by a circuit shown here in block diagram:



The 200kHz clock is divided down to 20kHz by a ÷10 counter. The MF 2^3 address line is used to trigger a one-shot which resets the ÷10 counter at the appropriate time. The 20kHz is then counted down by a ÷8 counter which gives MF 2^0, etc.

5.6 Time Event Monitor (TEM-4)

The TEM-4 shown in Figure 5.6.1 registers the time-of-occurrence for the leading edge of each of 4 input pulses. Each of the four circuits in the TEM-4, as shown in Figure 5.6.2, consists essentially of just a 9-bit latch which reads the state of the PCM address lines upon recognition of the leading edge of the input pulse. The contents of the latch are dumped onto the digital bus at the appropriate sample time for each circuit.

Because the TEM-4 needs the PCM address bus as its data input, it must always be placed physically below the PAC-16 (if a PAC-16 is used on the same stack), otherwise it would read the modified address lines which are meaningless in terms of time-sequential information.

Since the PCM address bus changes every 50μsec, the TEM-4 has a time resolution of 50μsec. Since it has memory, the TEM will hold the "time" information until it is updated, thus allowing a sampling rate of 1 sample (per TEM channel) per paragraph. To get the same time resolution in a continually-sampled system, the samples would have to be taken every 50μsec for each of the four channels for a total of 20,000 samples per second per channel. The TEM provides the 50μsec resolution with a sampling rate of 40 samples per second per channel, for a reduction of 500 to 1 in required sampling rate.

Naturally, with a sampling rate of 1 sample per 25 milliseconds (1/40th of a second) the input pulses must be at least 25 milliseconds apart. Since the TEM is normally used with very slow transducers (horizon sensors, etc.) this has not been found to be a limitation for any practical application of the TEM.

The data from the TEM, unfortunately, does not lend itself to "eyeball" data reduction, and in fact is generally incomprehensible to anything but a computer (or a very tedious hand analysis from a digital computer printout of the data). There is an existing computer program which is used to evaluate data from a TEM which has lunar-sensor (or horizon sensor) inputs. It is currently planned to develop a more general computer program for use with TEM data.

For the benefit of those experimenters who may wish to use the TEM with their own transducers, a brief explanation is given here of how to interpret the TEM data:

First, it is necessary to consider where in the paragraph the TEM data is sampled. For the sake of this example, we will assume that the TEM channel of interest is in 15-4-5. This is a realistic value since the TEM's are normally programmed for 15-x-5 with x = 4 through 11 (that leaves room for 8 TEM channels).

Since the data is sampled continually, the only way it can be determined that a pulse has entered the TEM is to observe a change in the channels data value.* The matrix index of 15-4-5 is (4-1) x 16 + 15 = 63. When a change is observed, the new value is then compared to the matrix index (63 in this case) of the channels data position. If the new value is greater than or equal to the index, then the pulse occurred during the previous paragraph but after the previous sample. If the value is less than the index, then the pulse occurred in the current paragraph and prior to the current sample. Figure 5.6.3 shows graphically how the true value is determined. As a further example of the use of the TEM, the distance between the two pulses of Figure 5.6.3 will now be calculated:

*This leads to an anomaly if the new data occurs at the same matrix position as the previous value. Resetting the TEM after a reading would not eliminate the problem, however, it simply moves the problem to matrix position Ø.

As shown in Figure 5.6.3, the pulses are "located" by comparing the data values with the matrix index. In this case, the number of words between pulses is

(511 - 200) + 3 paragraphs + 10

= 311 + 3 x (512) + 10

= 311 + 1536 + 10

= 1857

At 50μsec per word, this represents a pulse separation of .092850 seconds, ($\pm$50μsec RMS error).

In this example, a pulse separation of nominally 100 milliseconds was measured to within 0.05% accuracy. The absolute error remains $\pm$50μsec no matter how large the pulse separation, so large pulse separation, the relative (%) error becomes insignificant.

The calculations just described are obviously ideally suited to computerized data analysis, and it is anticipated that all final data reduction for TEM data will be computerized.

5.7 Remote Bi-Level Monitor (RBM-4)

This unit accepts up to 36 discrete bi-level inputs (4 words). It contains four identical and independent bi-level channels. The electrical interface is essentially the same as in the bit monitor of the ASC-32 module where overvoltage protection is provided. The digital data is transferred to a parallel to serial converter at the coincidence of address and data transfer pulses. The timing diagram is shown in Figure 5.7.3. The selected channel is addressed one word time slot earlier. The data is outputted in serial form to the digital module (DAM-1) where they are converted and strobed in parallel form to the PCM data bus at the selected channel time by data transfer pulses. Bi-level inhibit signals are provided to the experimenter.

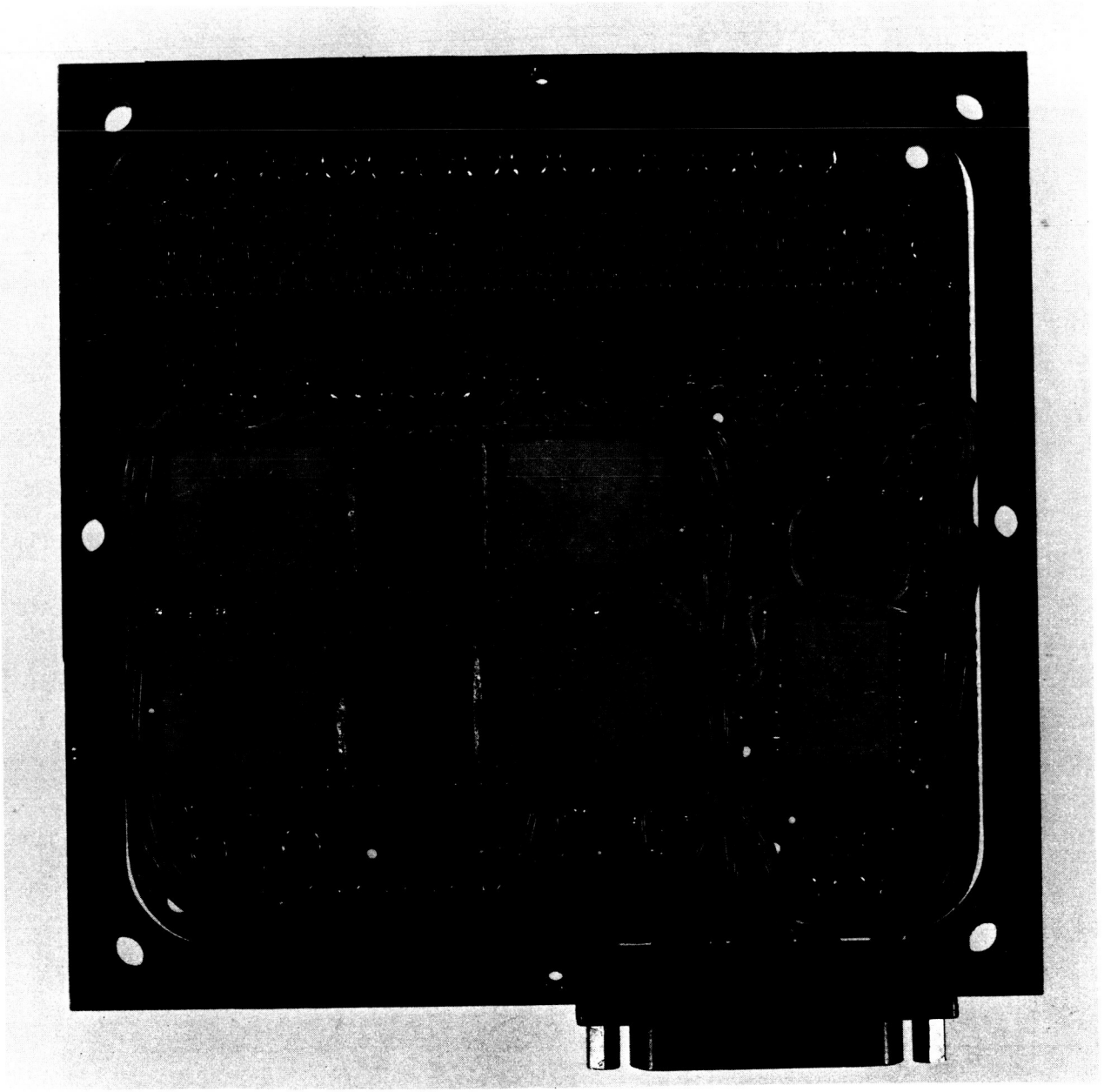


Figure 5.1.1. AS–32

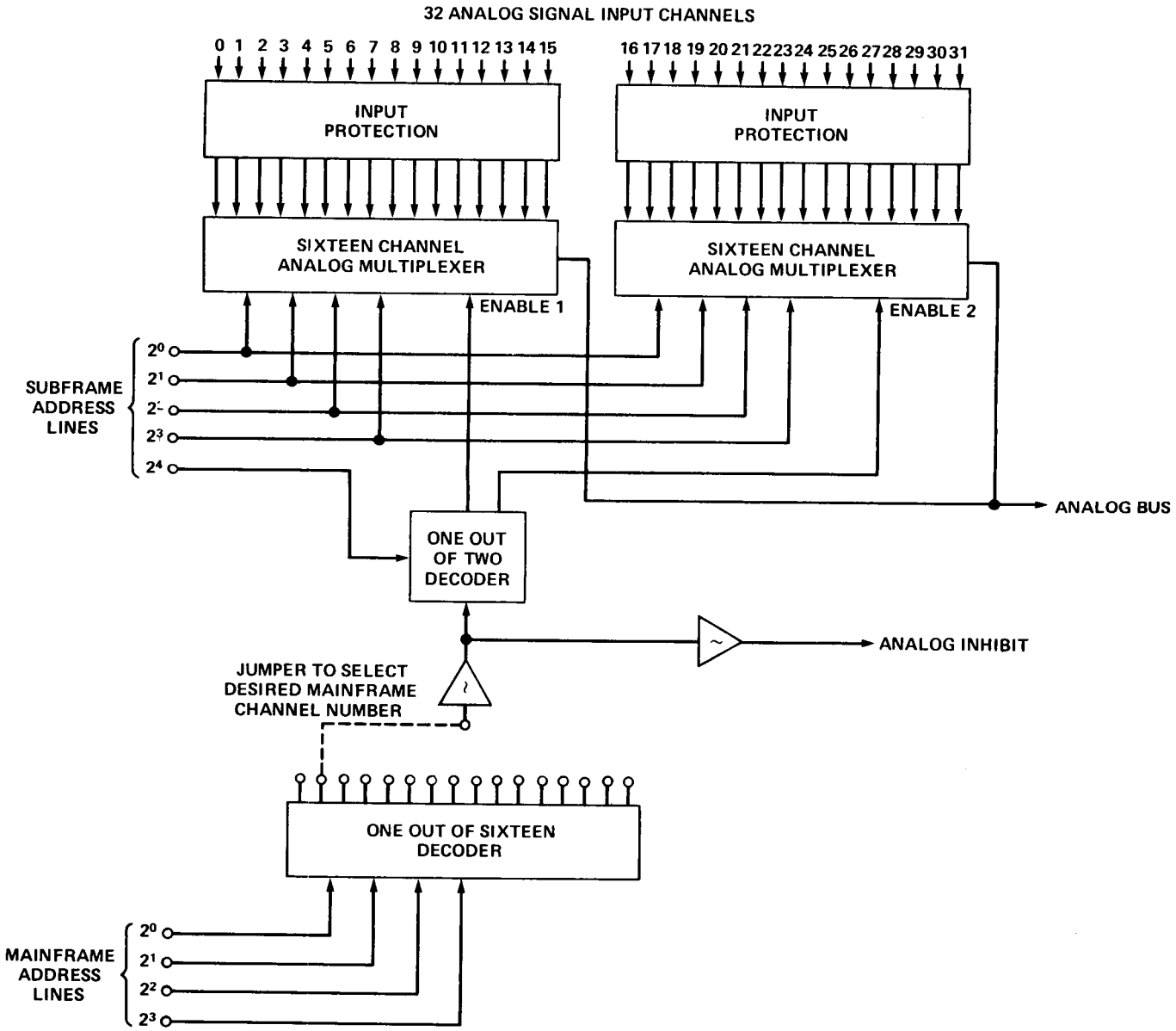


Figure 5.1.2. AS-32 Block Diagram

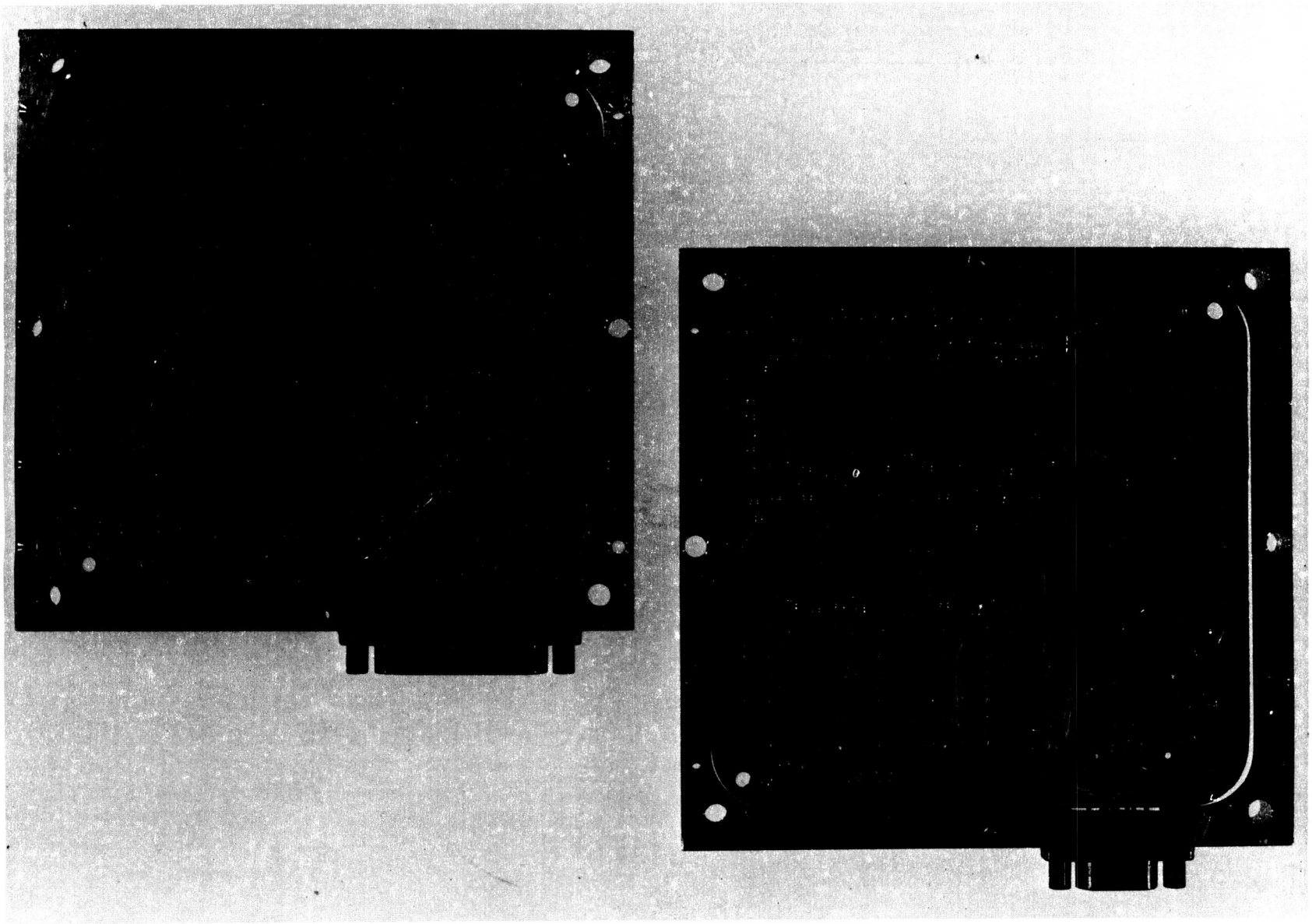


Figure 5.2.1. ASC-32

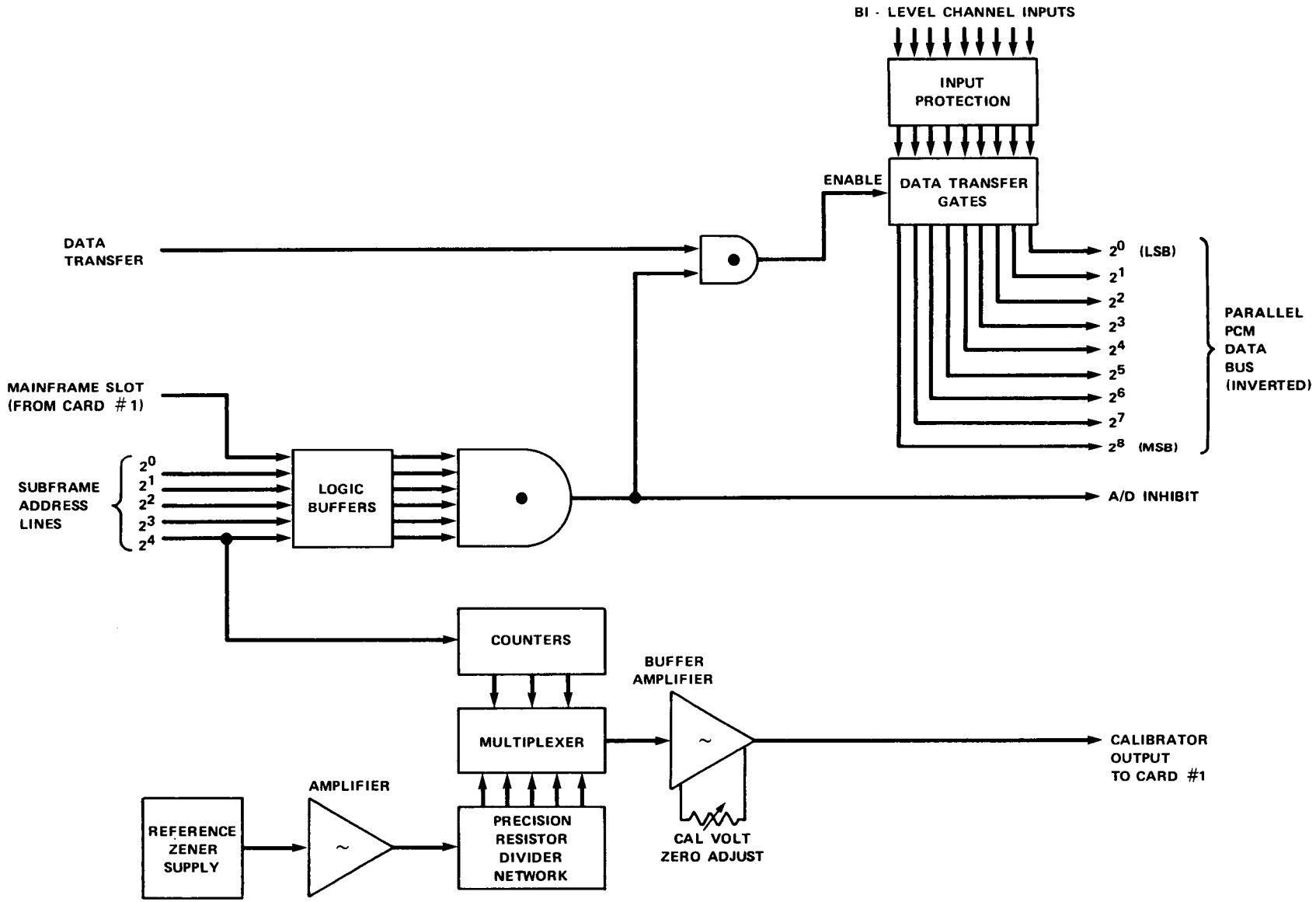


Figure 5.2.3. ASC-32 Calibration and Bi-Level Monitor Block Diagram

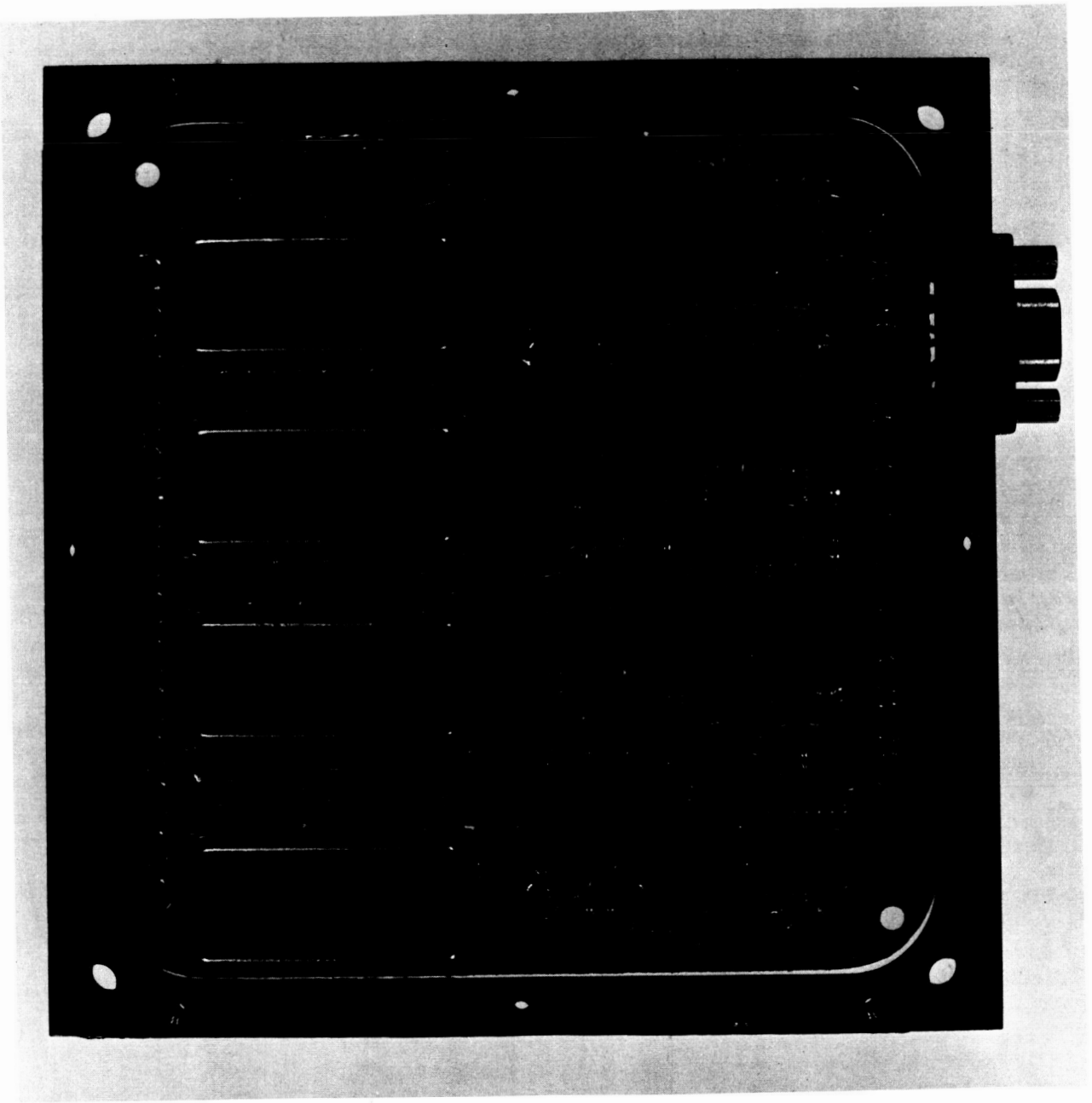


Figure 5.3.1. RCM-4

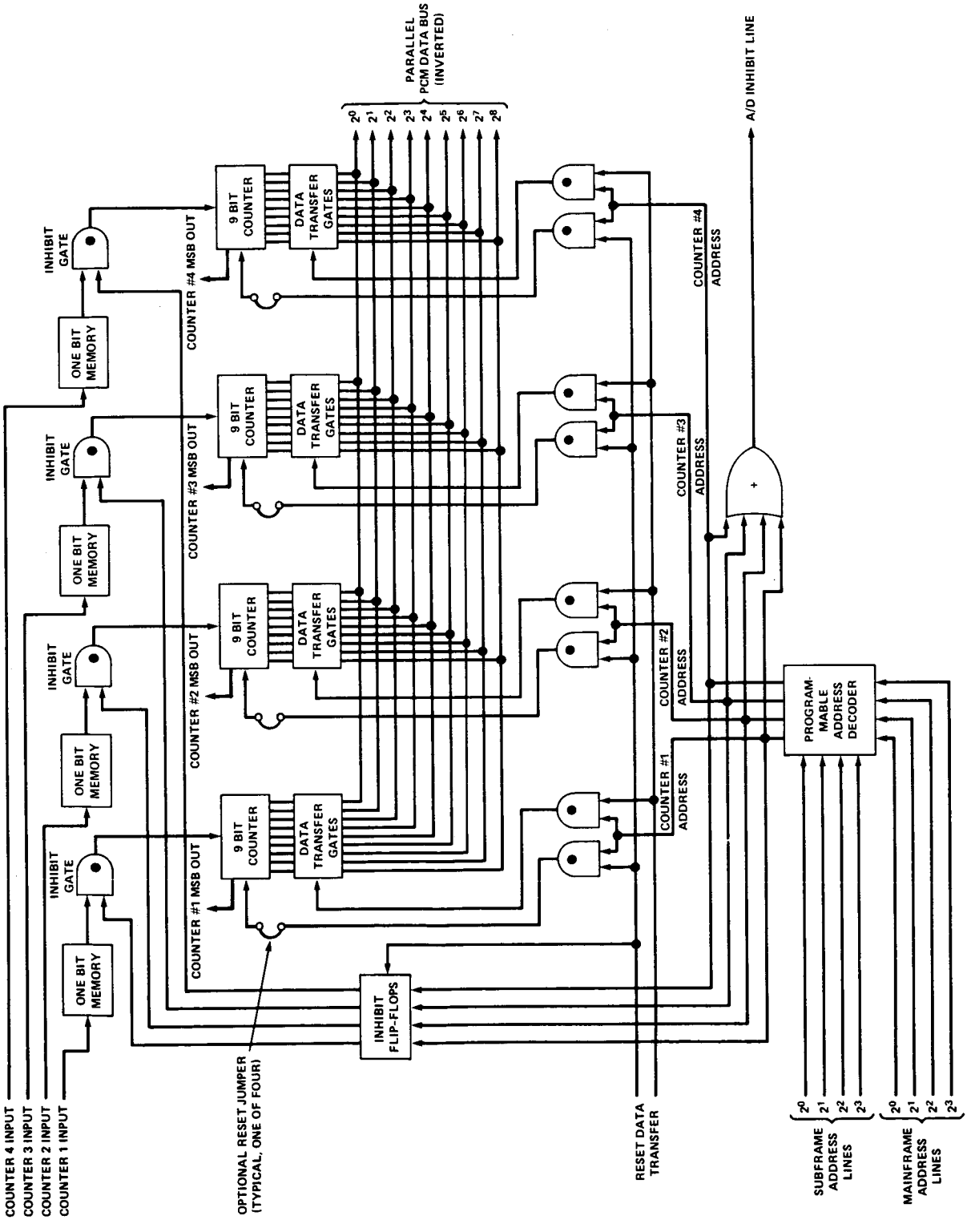


Figure 5.3.2. RCM-4 Block Diagram

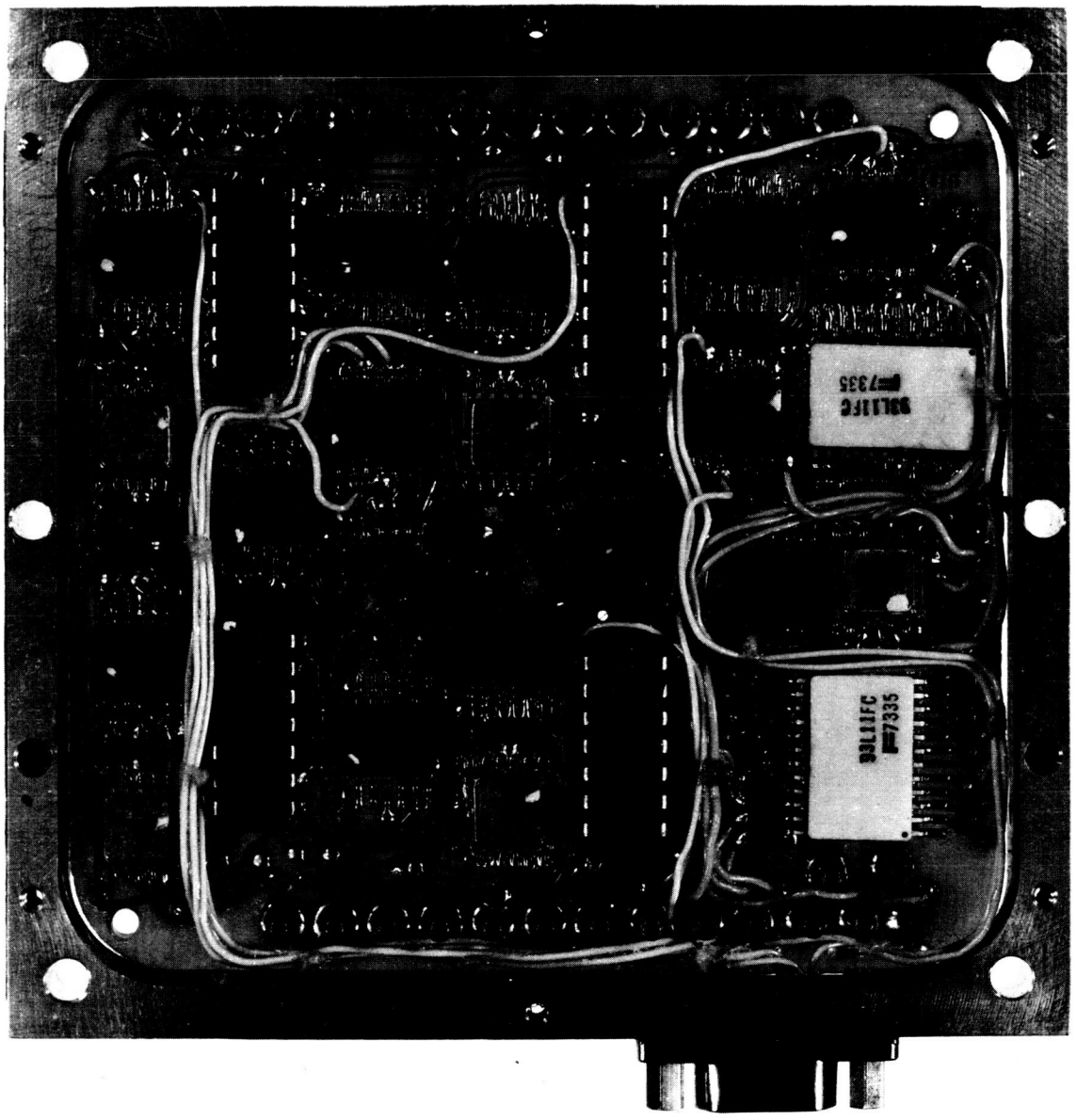


Figure 5.4.1.1. SIDL-8

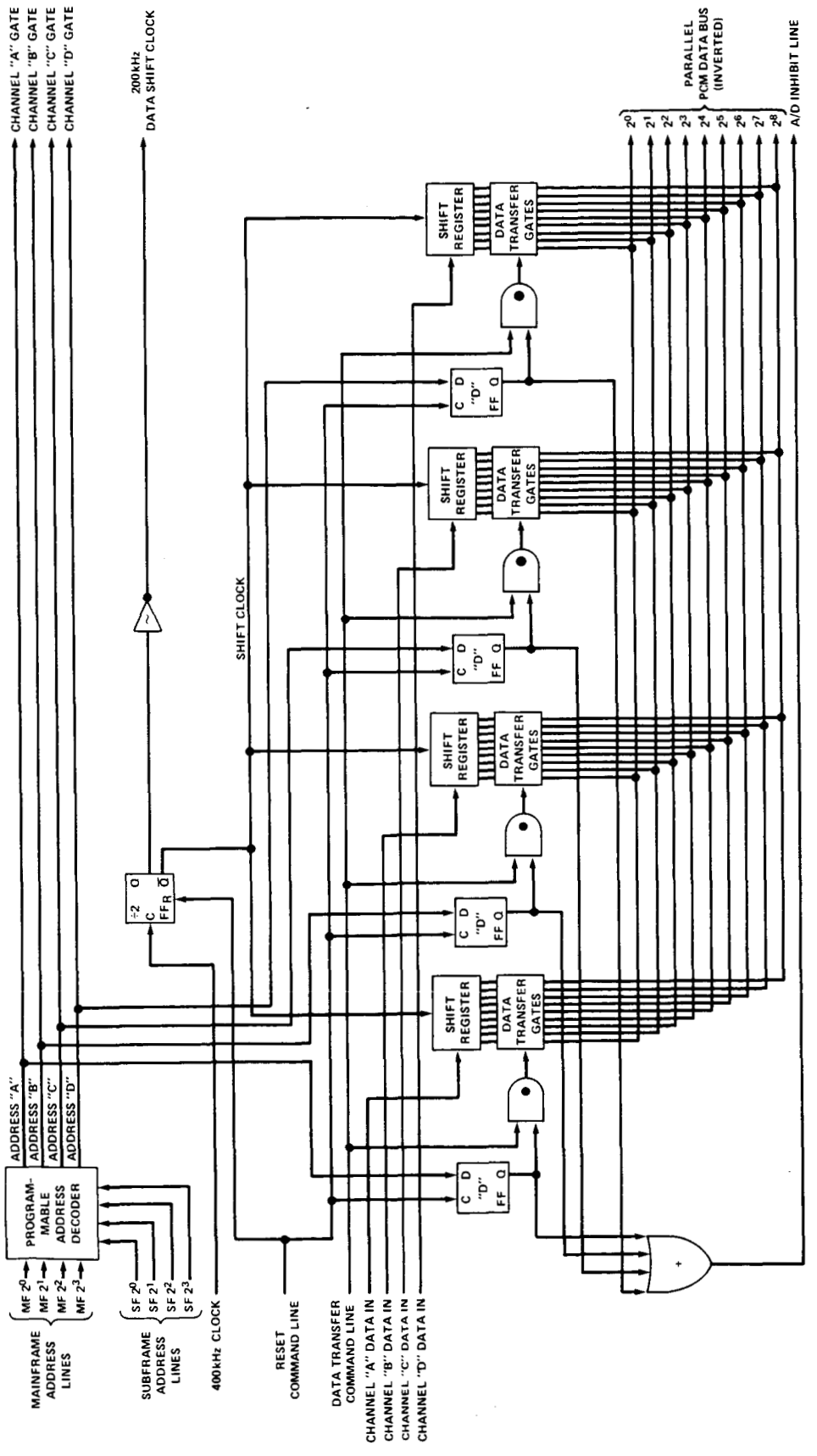


Figure 5.4.1.2. SIDL-8 Block Diagram

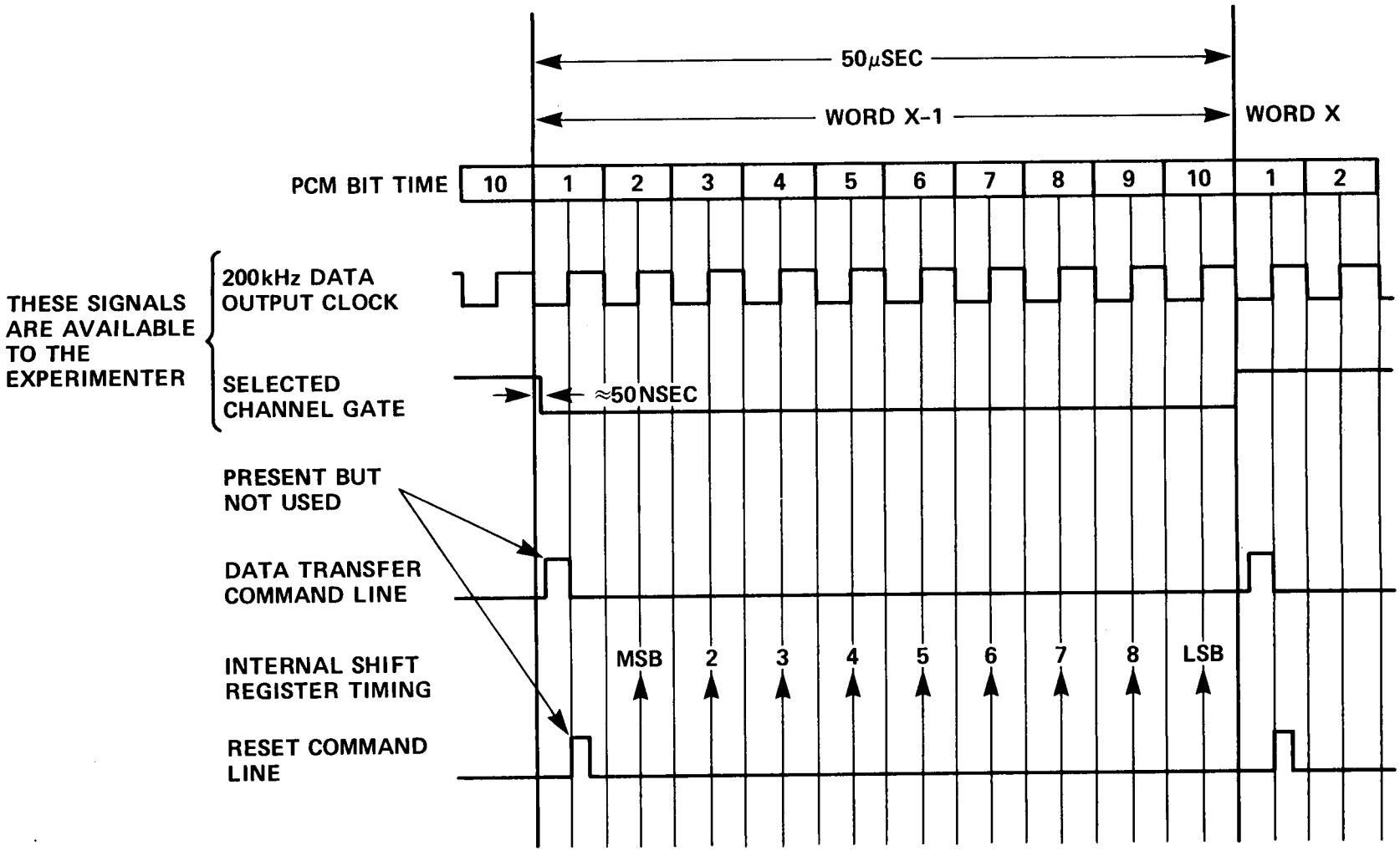


Figure 5.4.1.3. SIDL-8 Timing Diagram

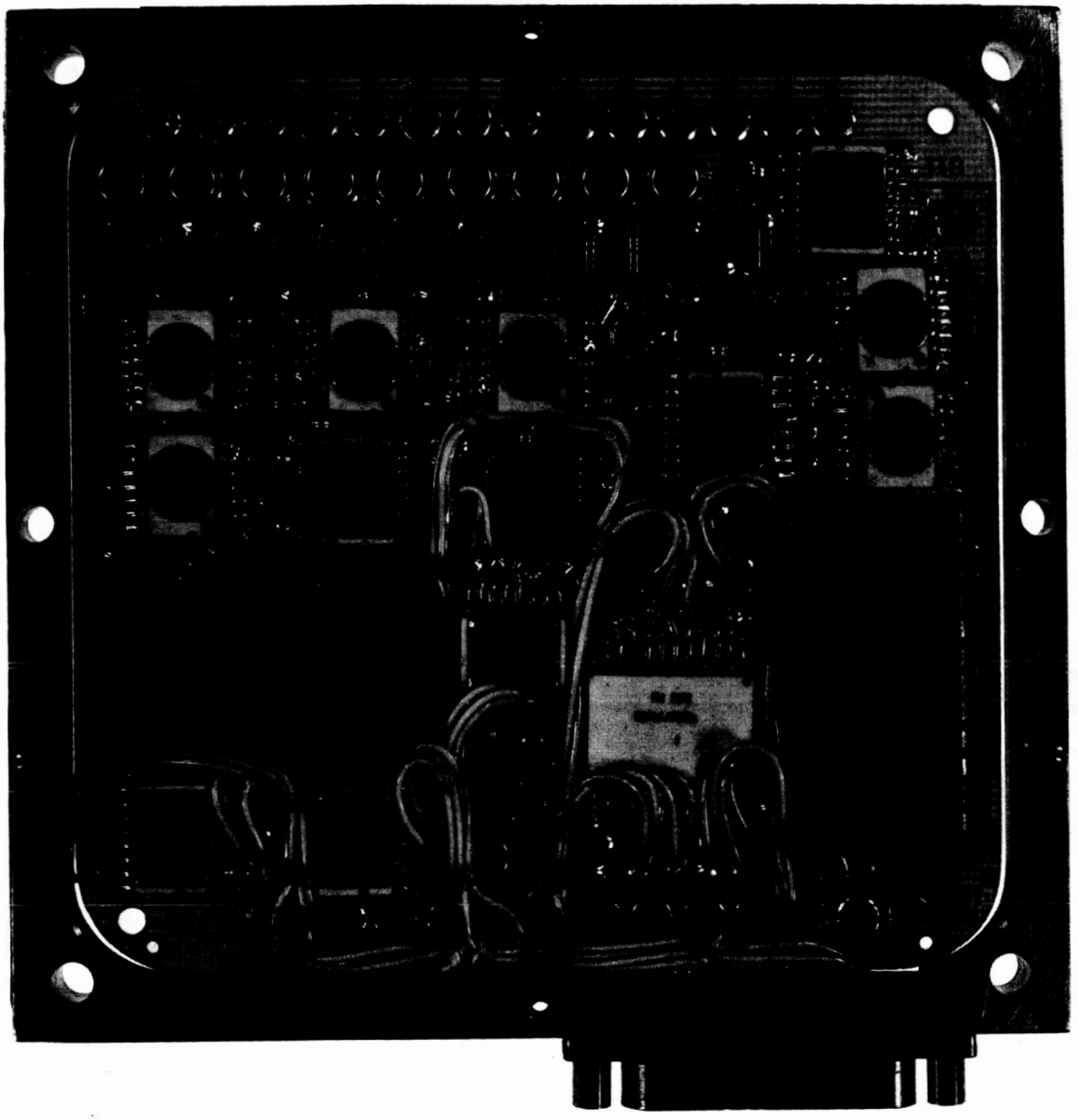


Figure 5.4.2.1. SIDL-16

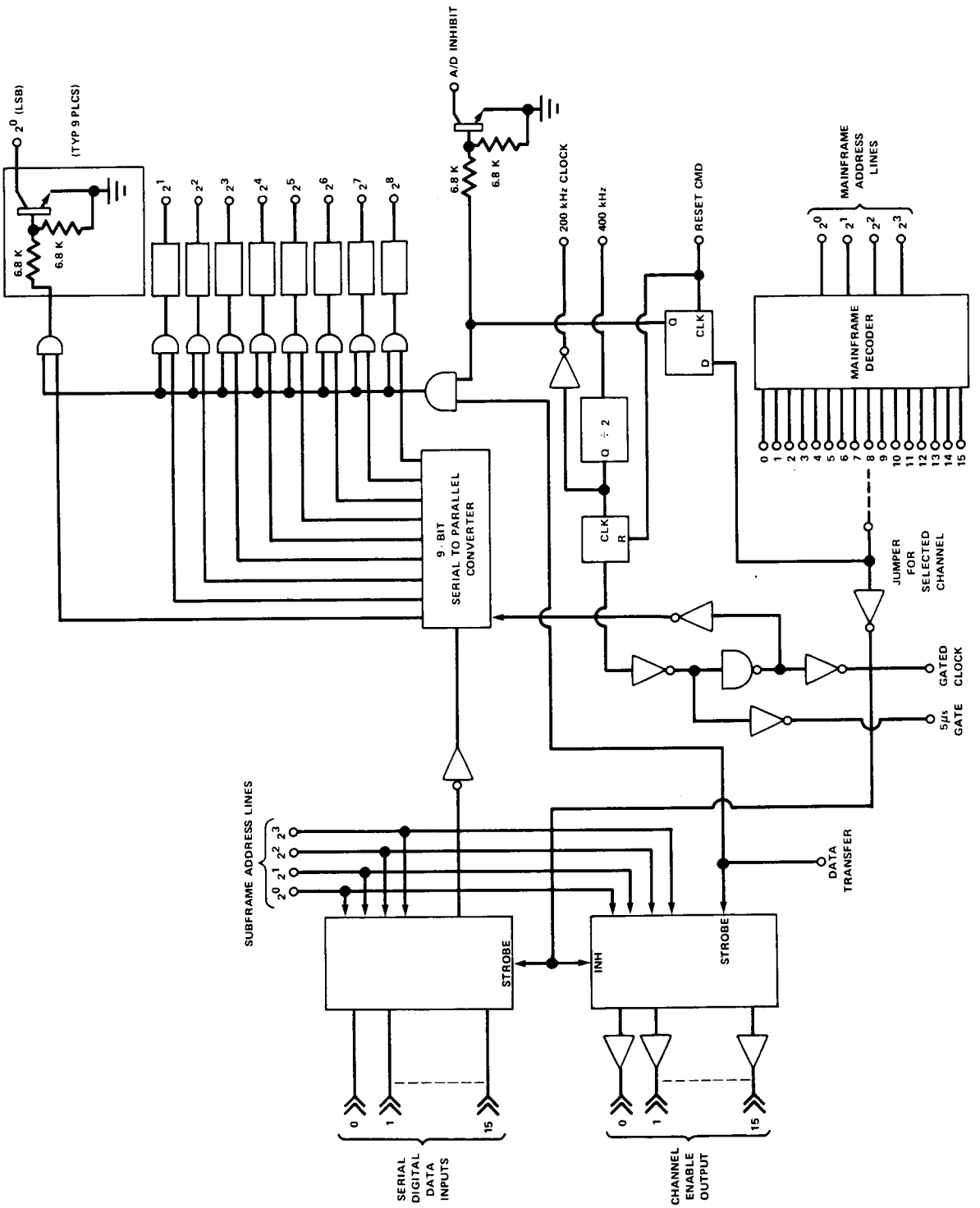


Figure 5.4.2.2. SIDL-16 Block Diagram

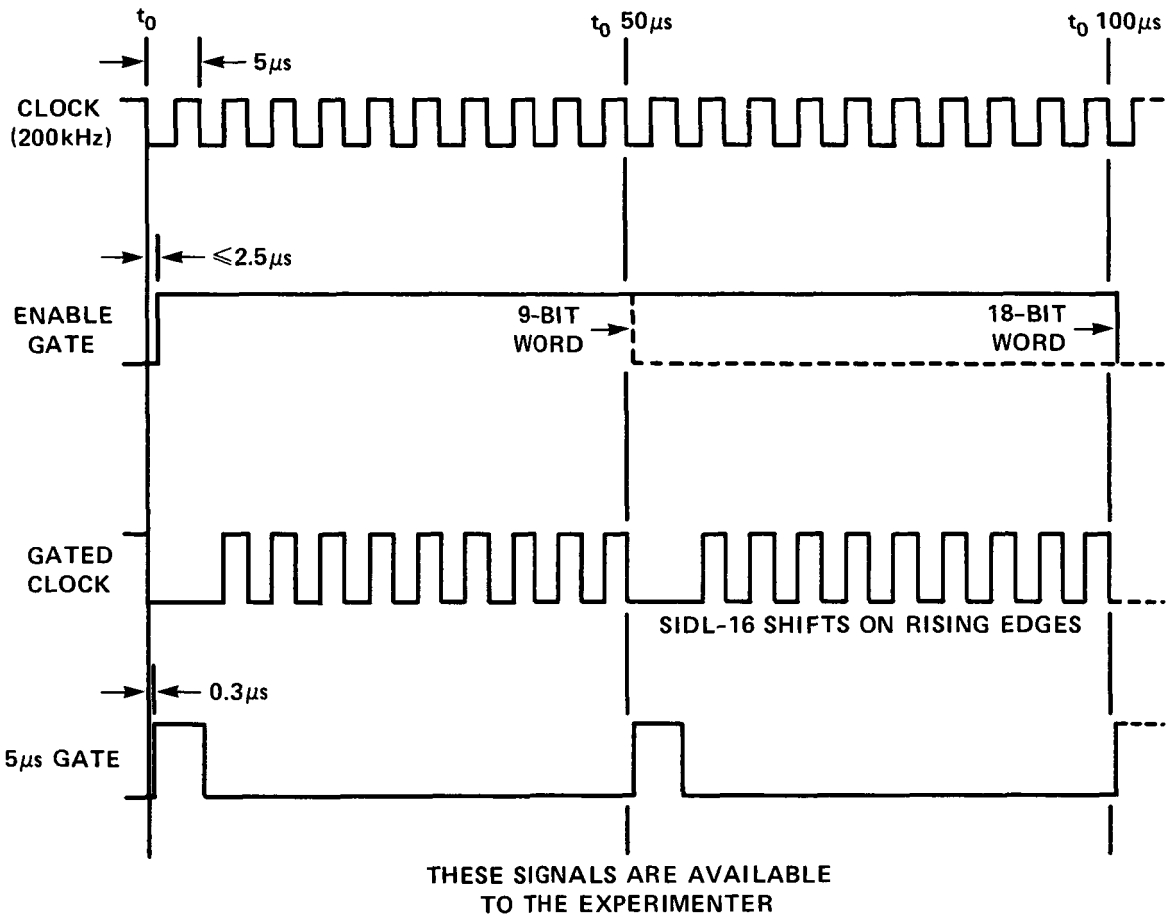


Figure 5.4.2.3. SIDL-16 Timing Diagram

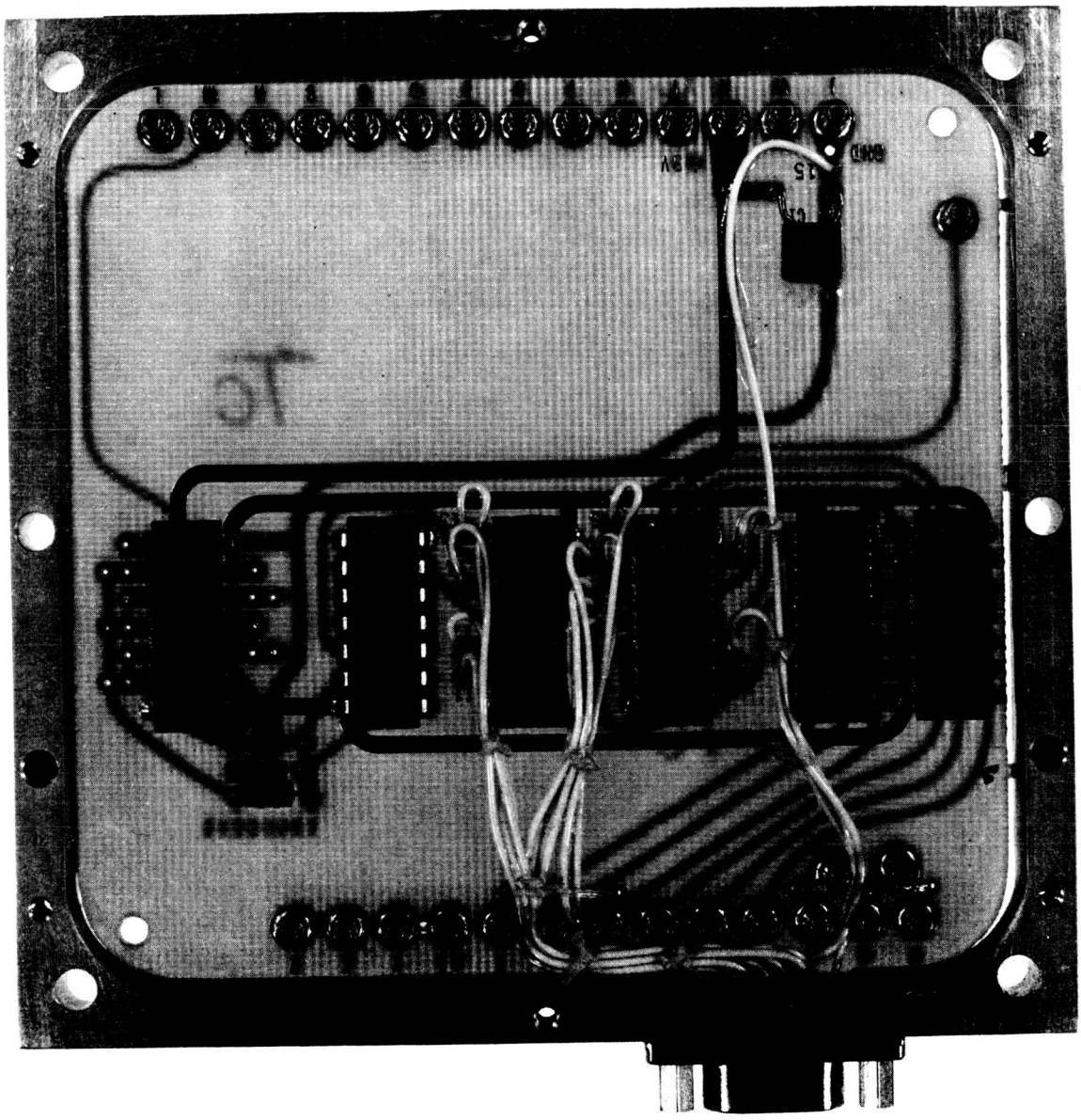


Figure 5.5.1. BUF-4

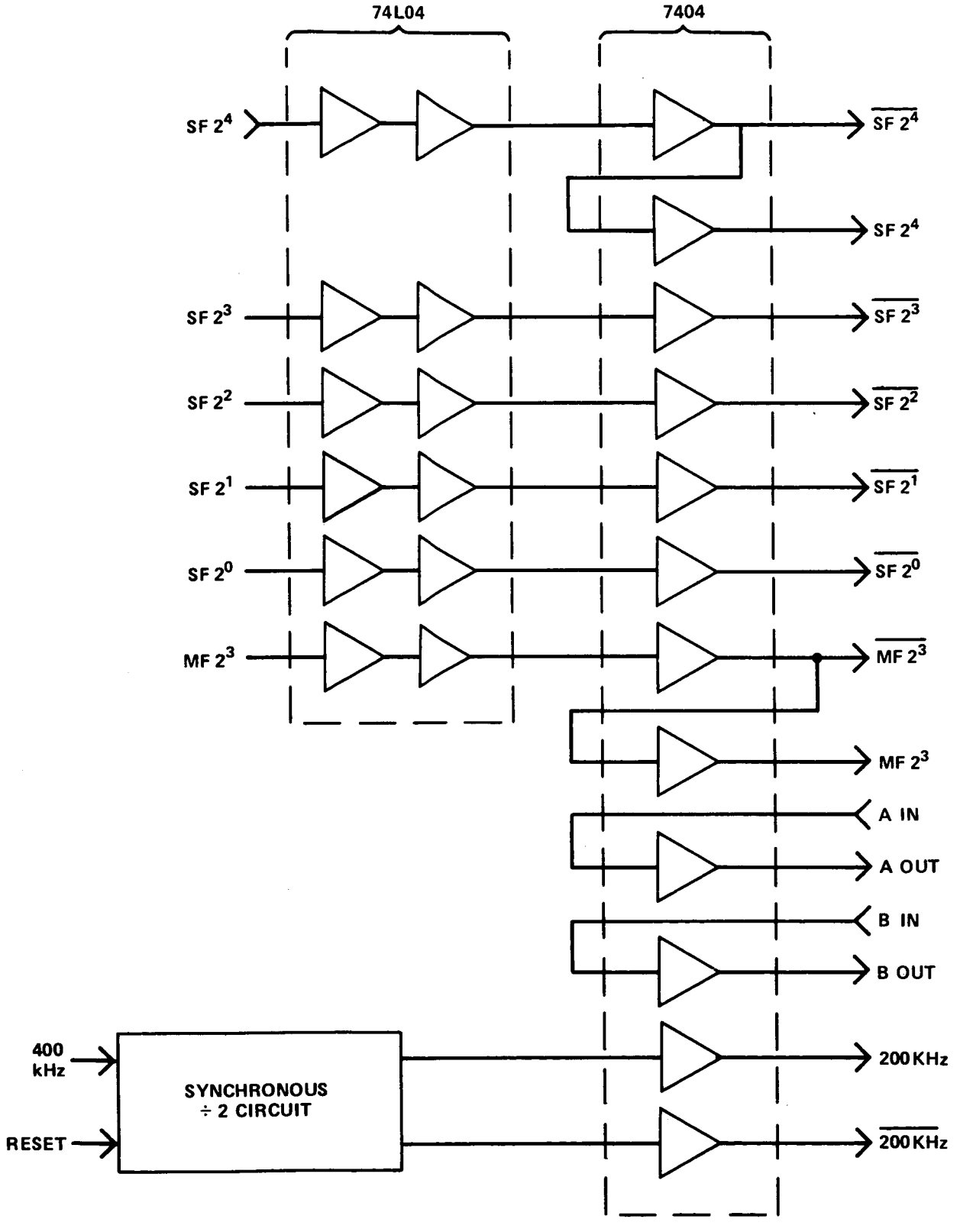


Figure 5.5.2. BUF-4 Block Diagram

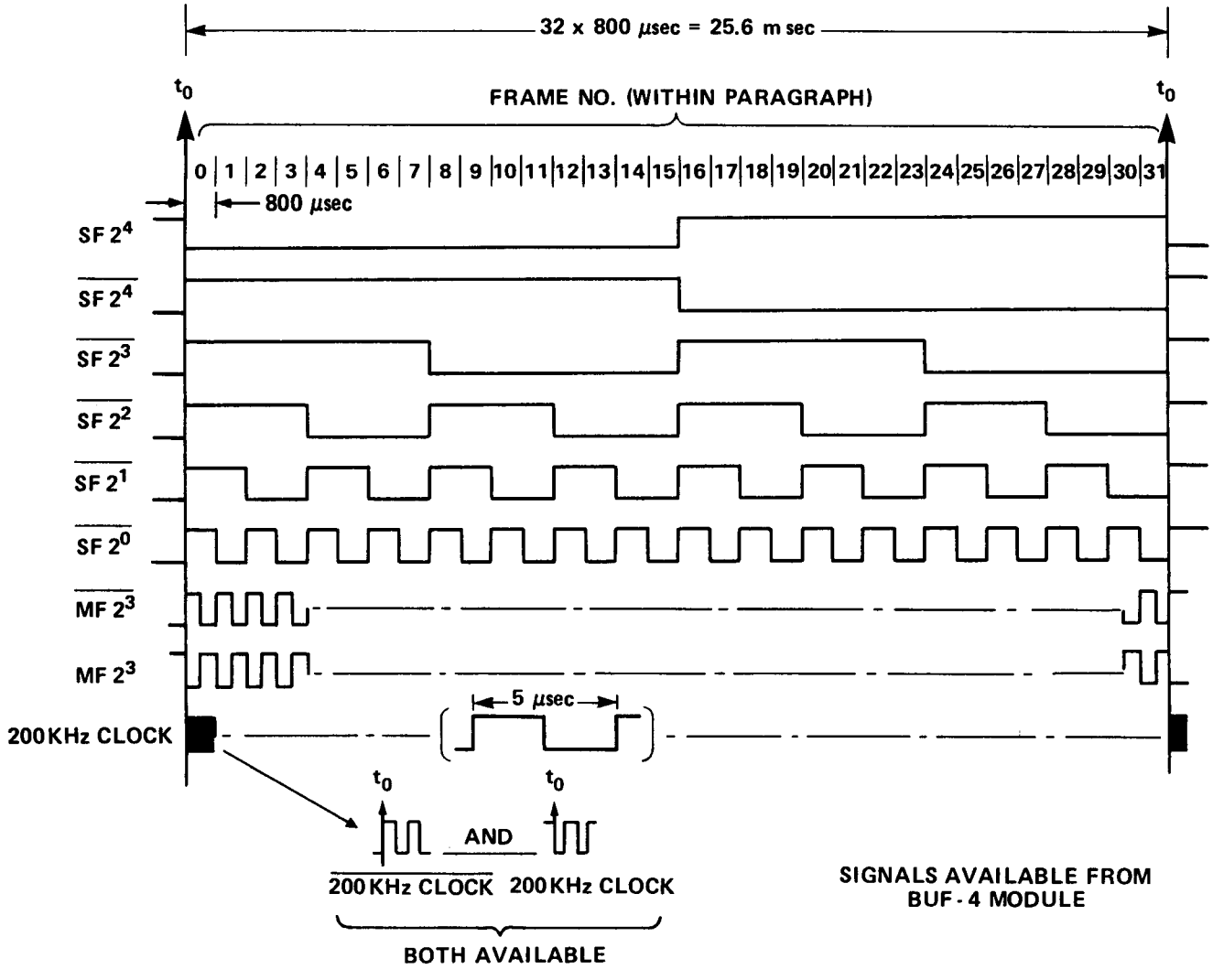


Figure 5.5.3. BUF–4 Timing Diagram

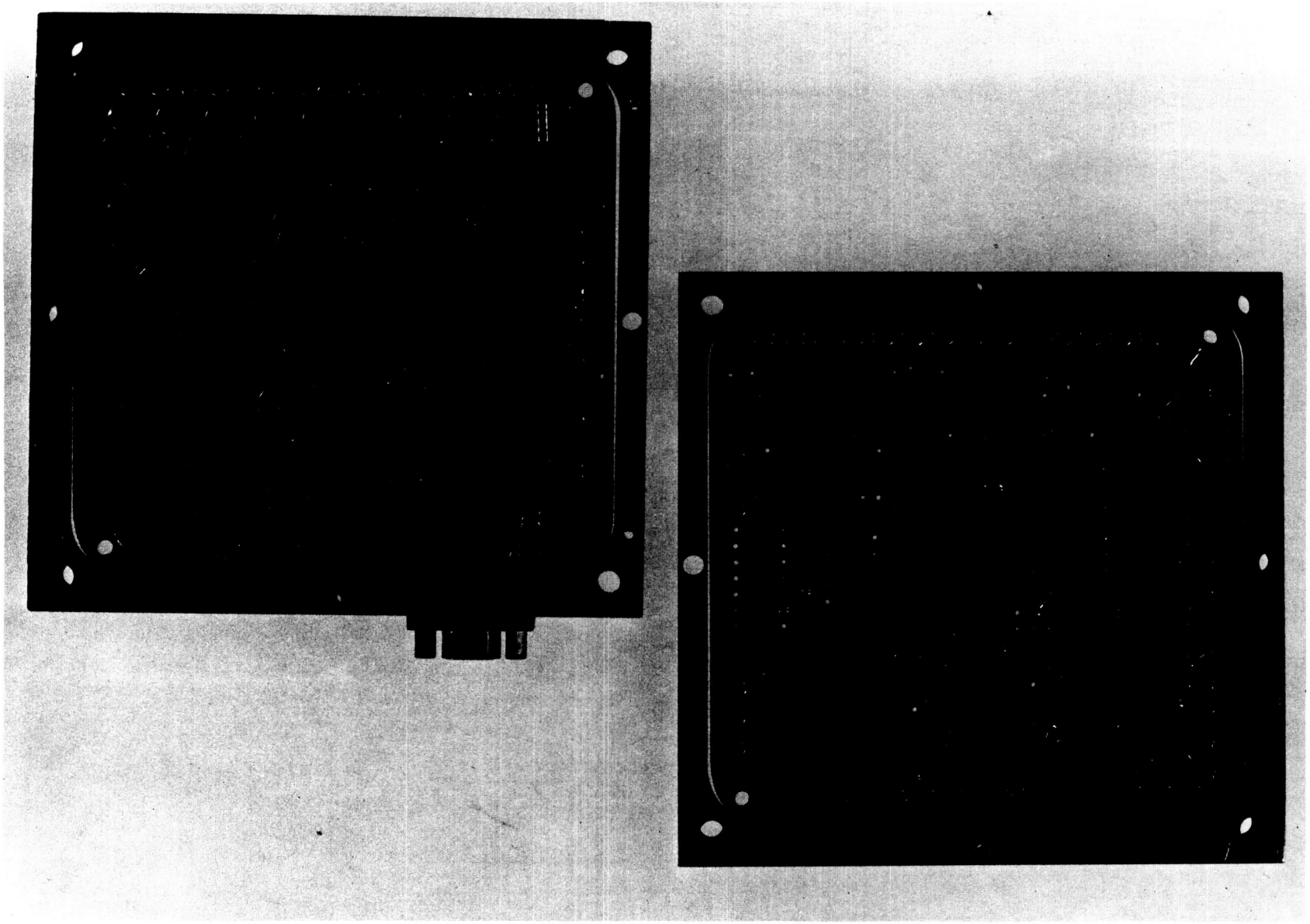


Figure 5.6.1. TEM-4

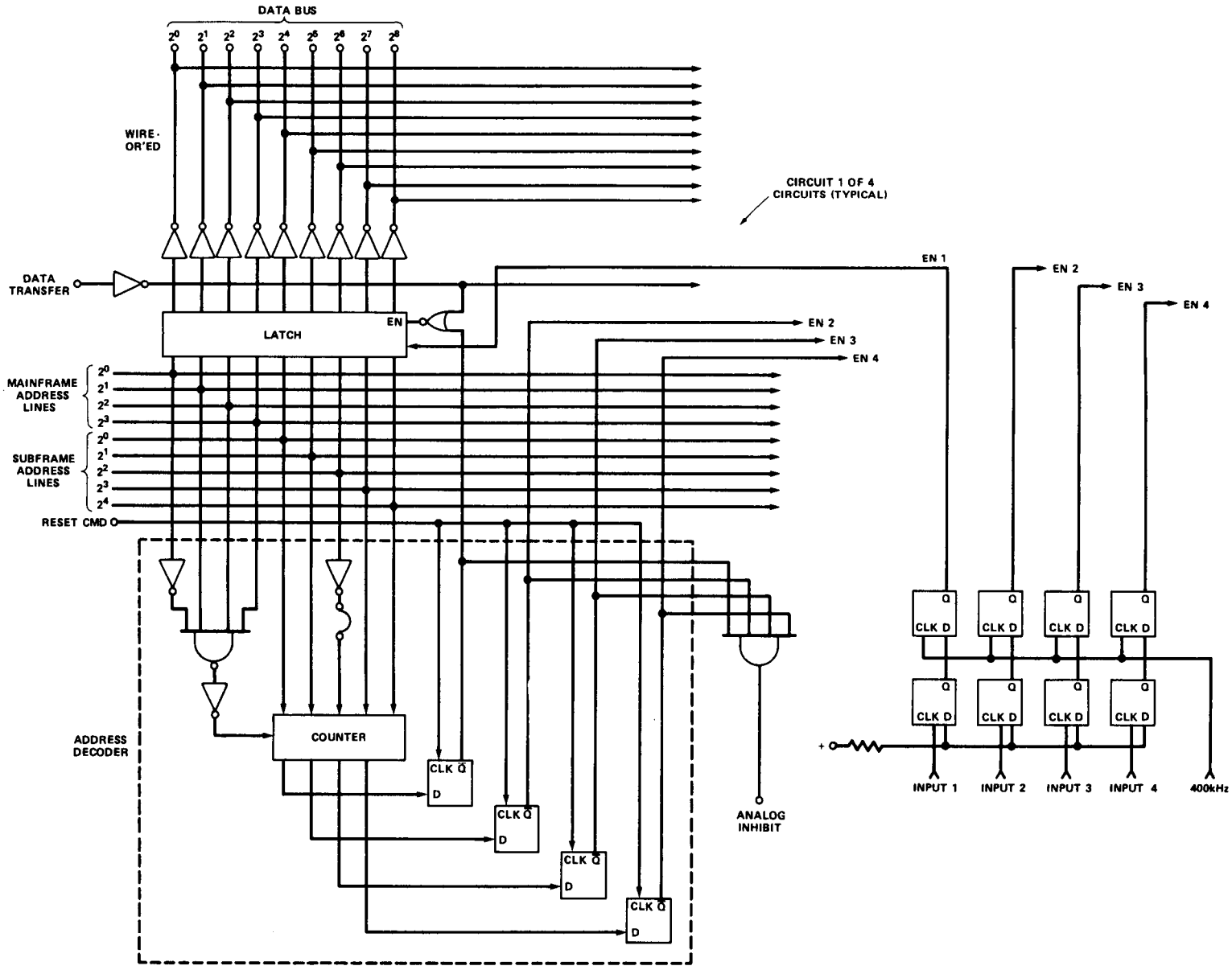


Figure 5.6.2. TEM–4 Block Diagram

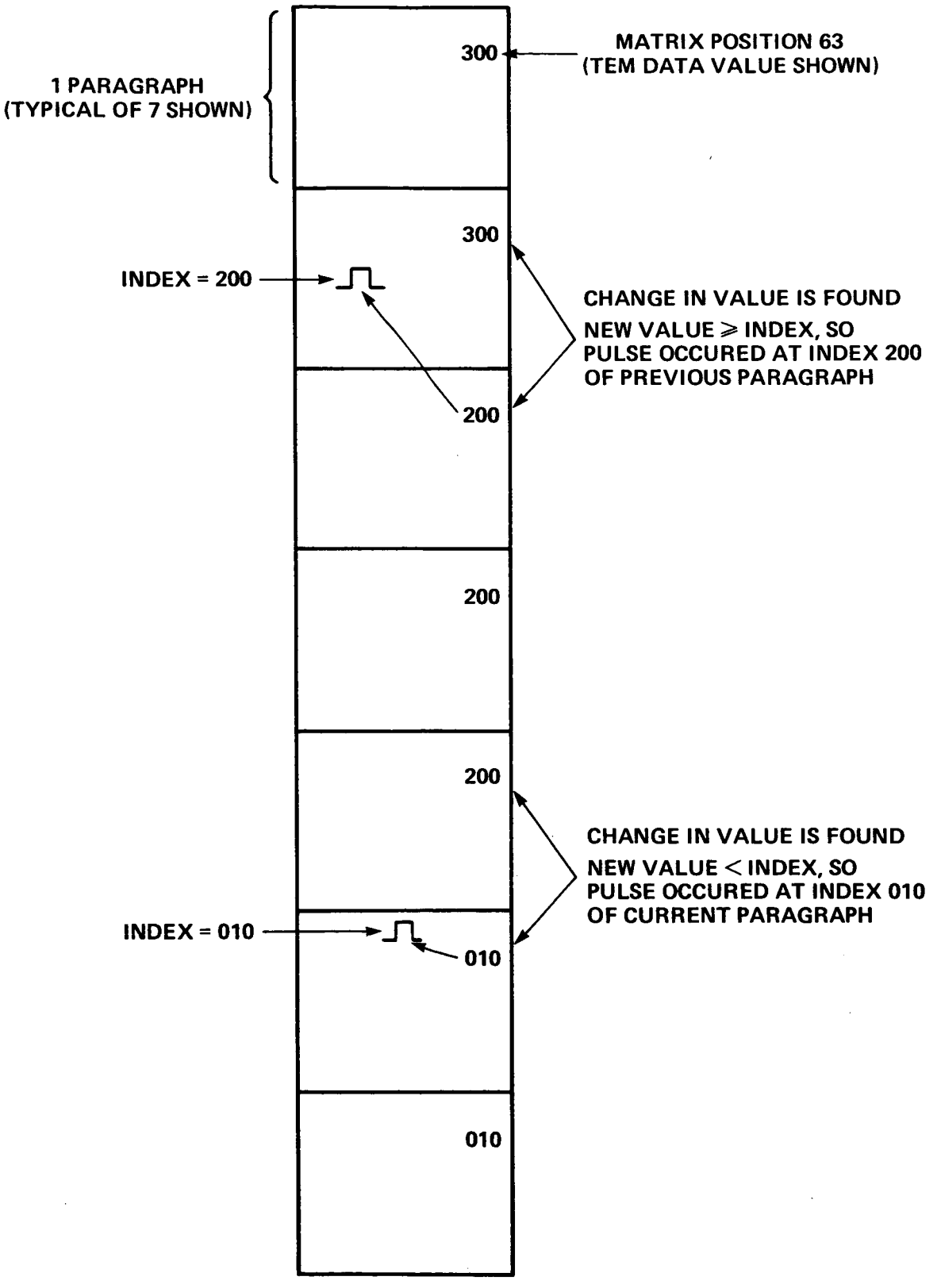


Figure 5.6.3. TEM–4 Data Calculations

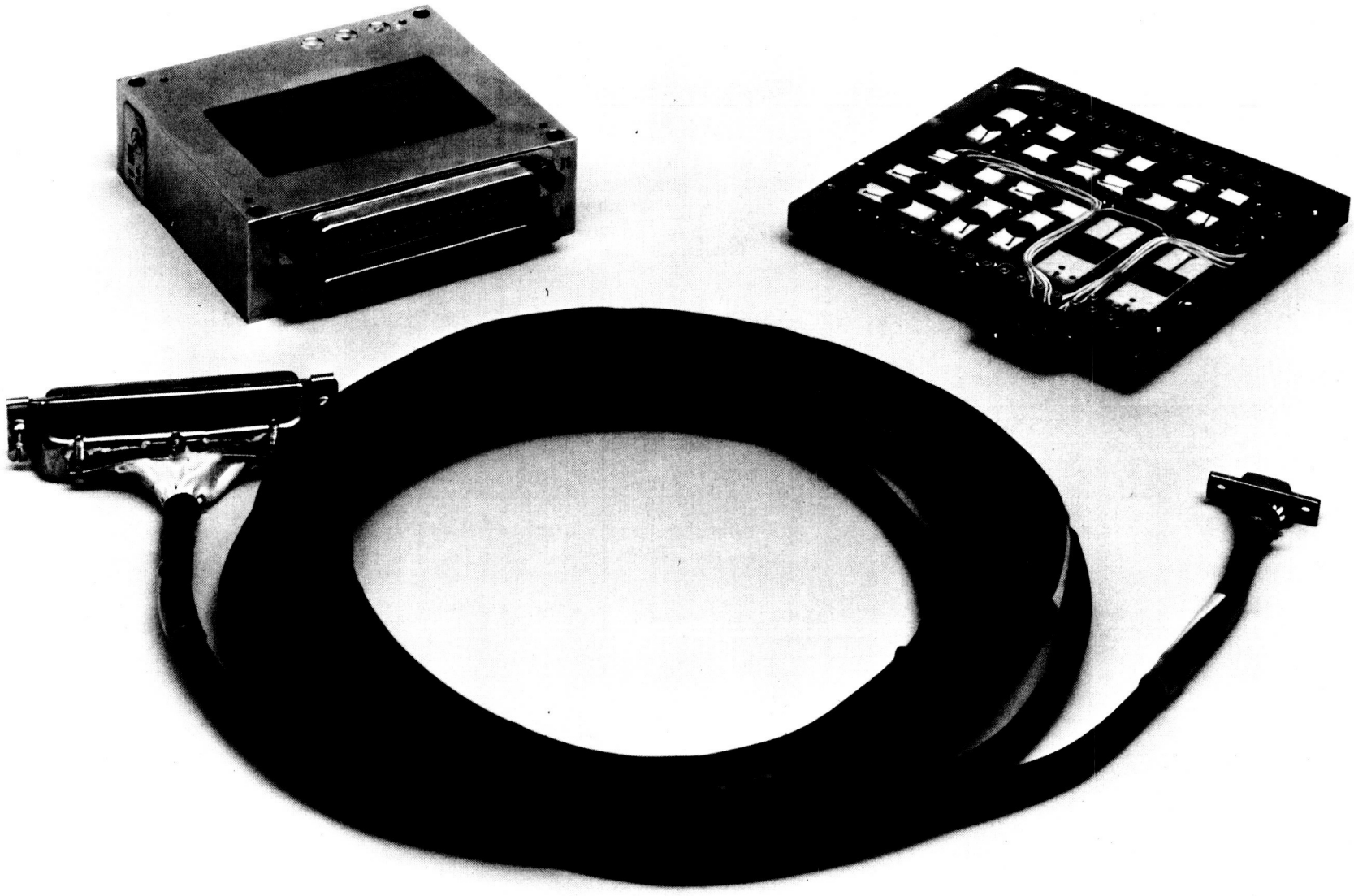


Figure 5.7.1. RBM-4

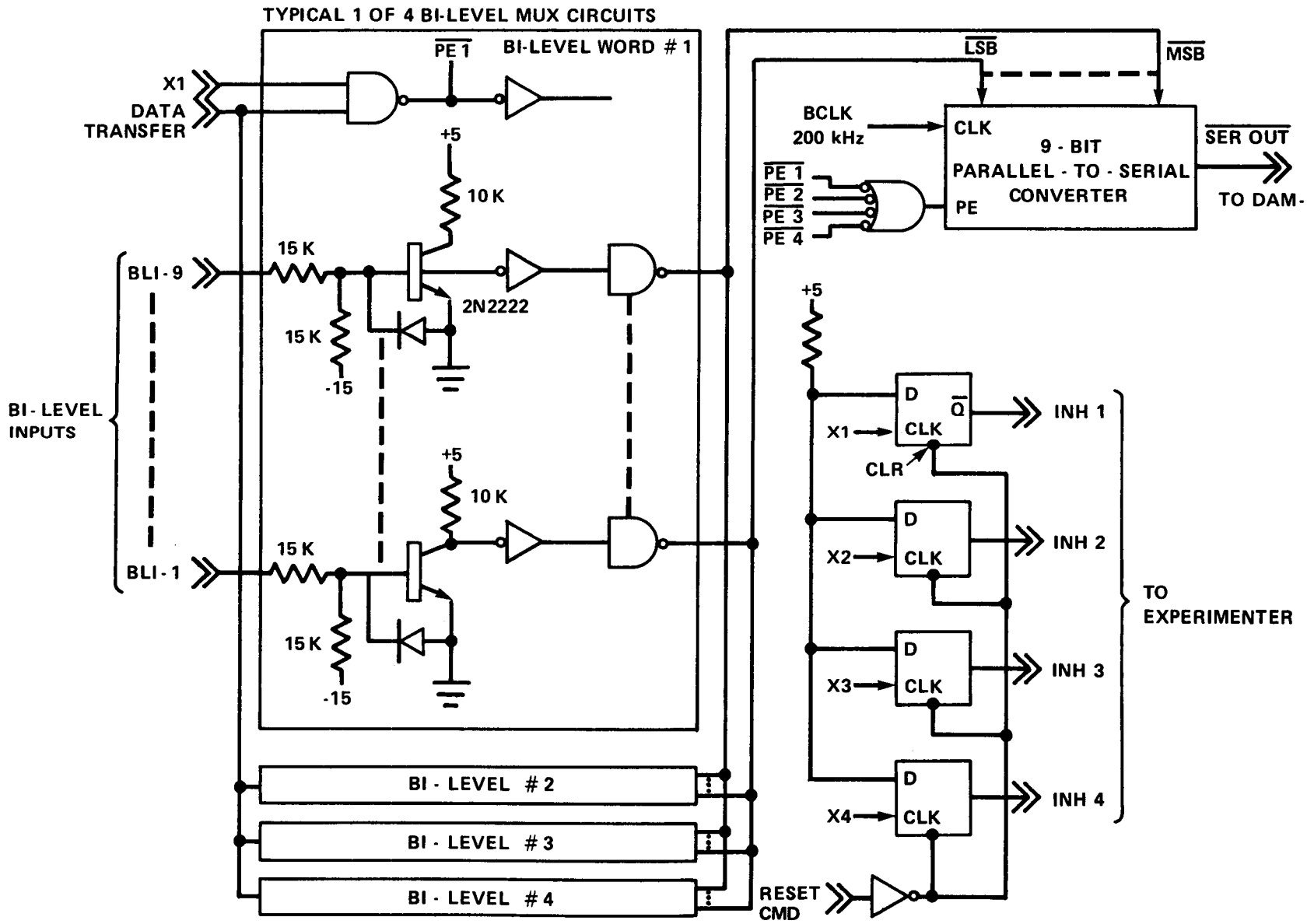


Figure 5.7.2. RBM-4 Block Diagram

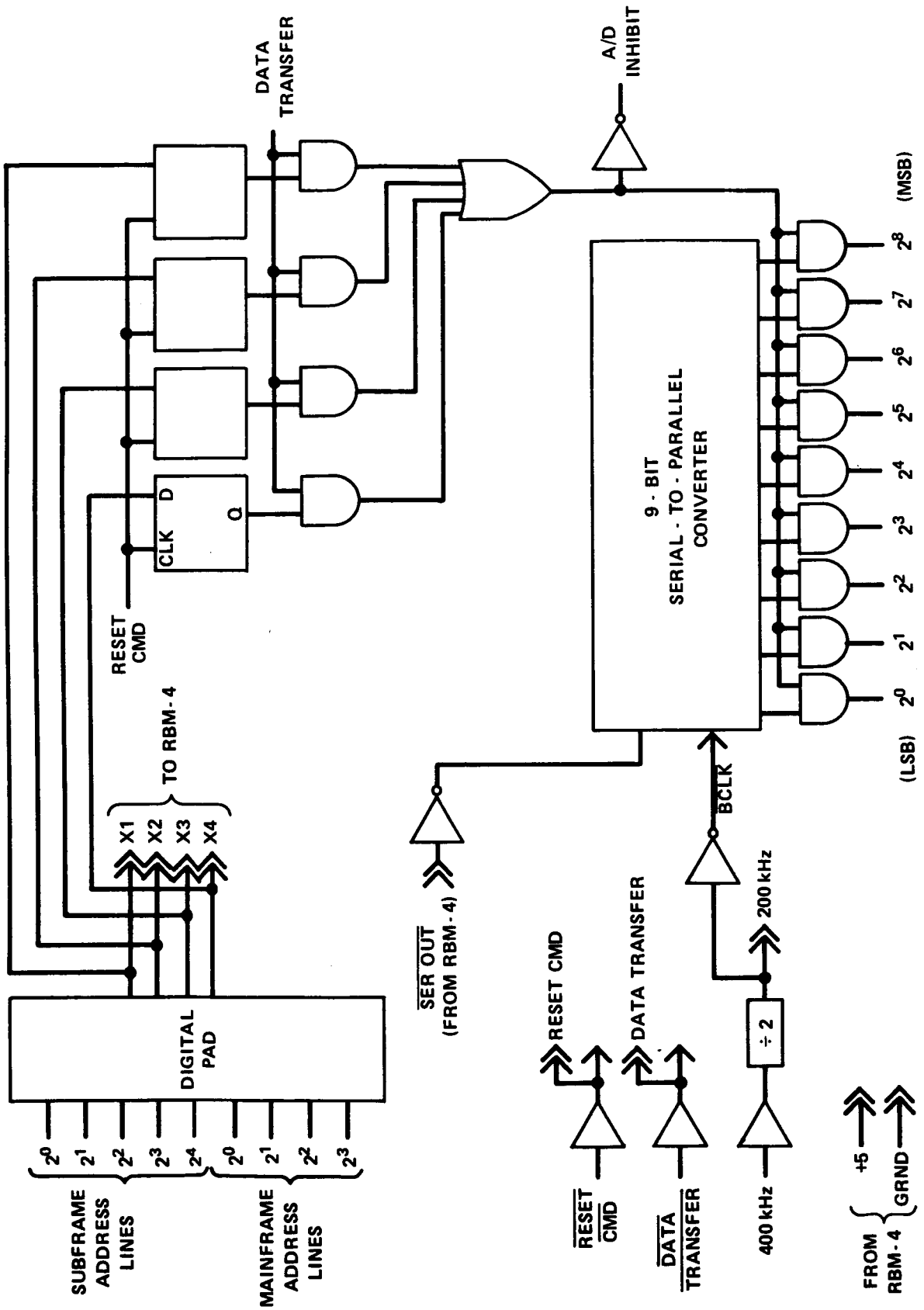


Figure 5.7.3. DAM-1 Block Diagram

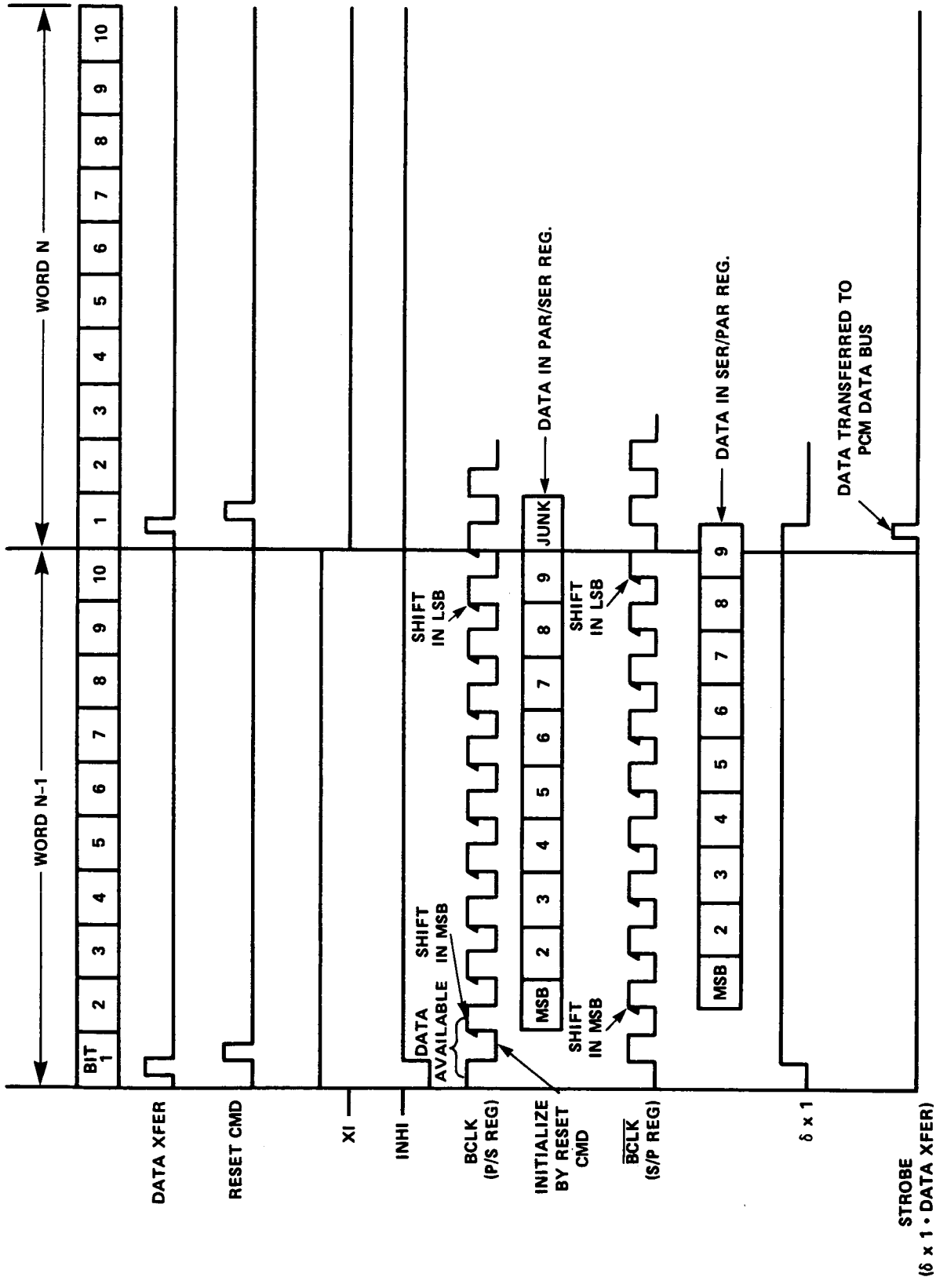


Figure 5.7.4. RBM-4 Timing Diagram

6.0 Booster Power Supply (BPS-5)

Data modules can be stacked on top of the SRT/MF (and each other) until physical or electrical limits are reached. The physical limits are governed by the particular mechanical arrangements of a given payload; inter-deck height (or deck diameter if the PCM stack is to be mounted on its side) is the limiting factor. The electrical limit is the current drain from the +5 V power supply in the SRT/MF. The mainframe power supplies residual +5 V current that is available for use by the expansion modules is 400 milliamperes, and the modules use various amounts of current at +5 V (details in Section 7.0).

When either the physical or electrical limits are exceeded by the "main stack" (the SRT/MF and the modules stacked directly on it) then some of the modules can be put on a "Booster Stack" starting with a BPS-5. The BPS-5 has an adapter board which connects it to the main stack. The adapter goes on the very top of the main stack. The booster stack has physical and electrical limits similar to those for the main stack. If the booster stack reaches its limits, a second booster stack can be started by putting a BPS-5 adapter on top of the first booster stack and then starting the second booster stack with another BPS-5. Similarly, a third booster stack could be added, however, it has never been necessary to use a third booster stack and even a second booster stack has been used only a few times in six years of flying these systems. Even the first booster stack is necessary on less than a third of all systems.

The BPS-5 provides only +5V to its modules. The other system voltages (±12, -27 Vdc) come from the SRT/MF. The packaging arrangement using one BPS-5 is shown in Figure 7.0. The BPS-5 itself is shown in Figures 6.1 and 6.2. The BPS-5 contains a synchronous chopper power supply (similar to the SRT/MF power supply) which runs from the 10kHz clock provided by the SRT/MF. In the case of a 50MHz SRT/MF, the 10MHz is provided by the PAC-16 as shown in Figure 4.3.2.

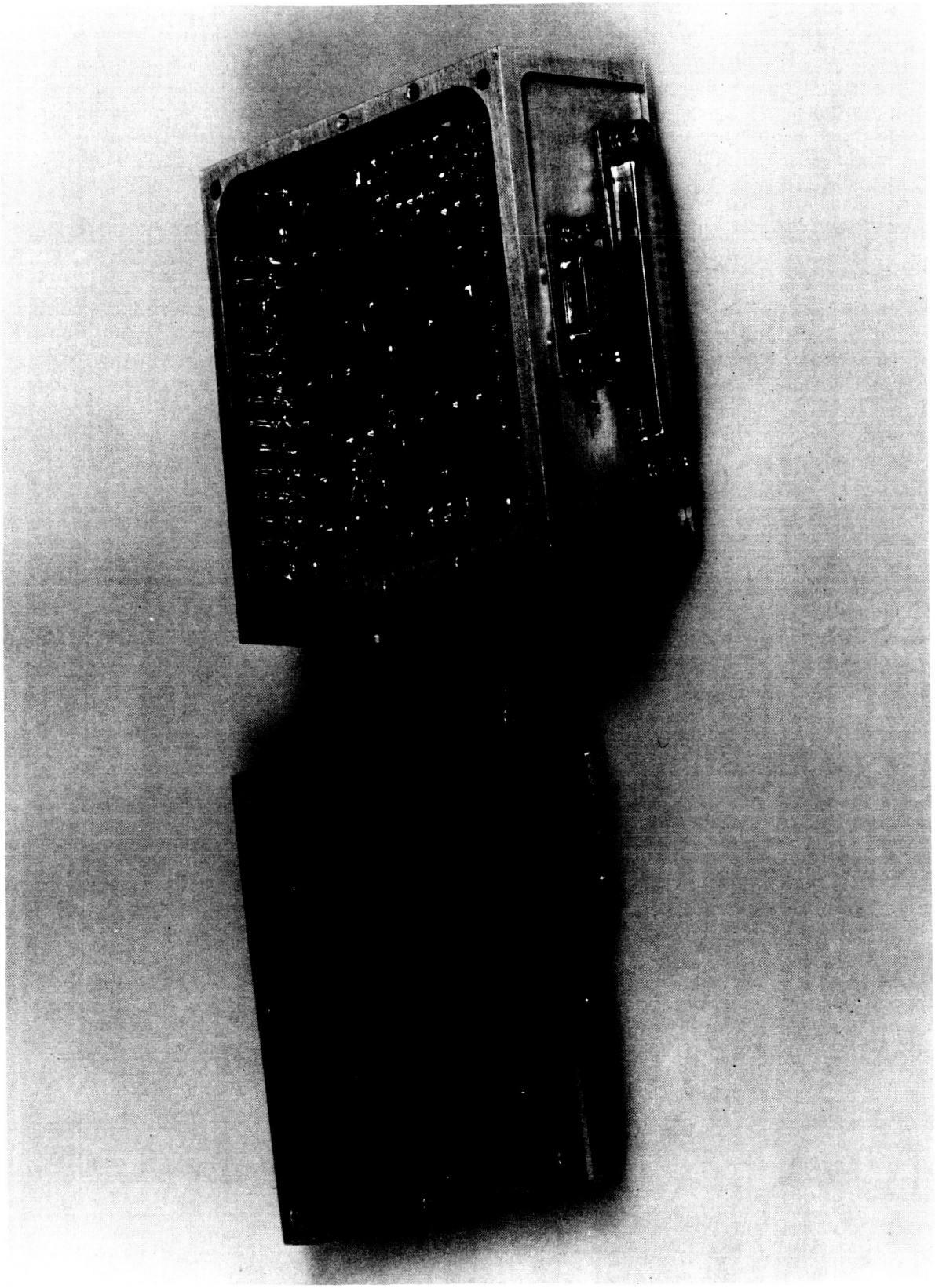


Figure 6.1. BPS-5

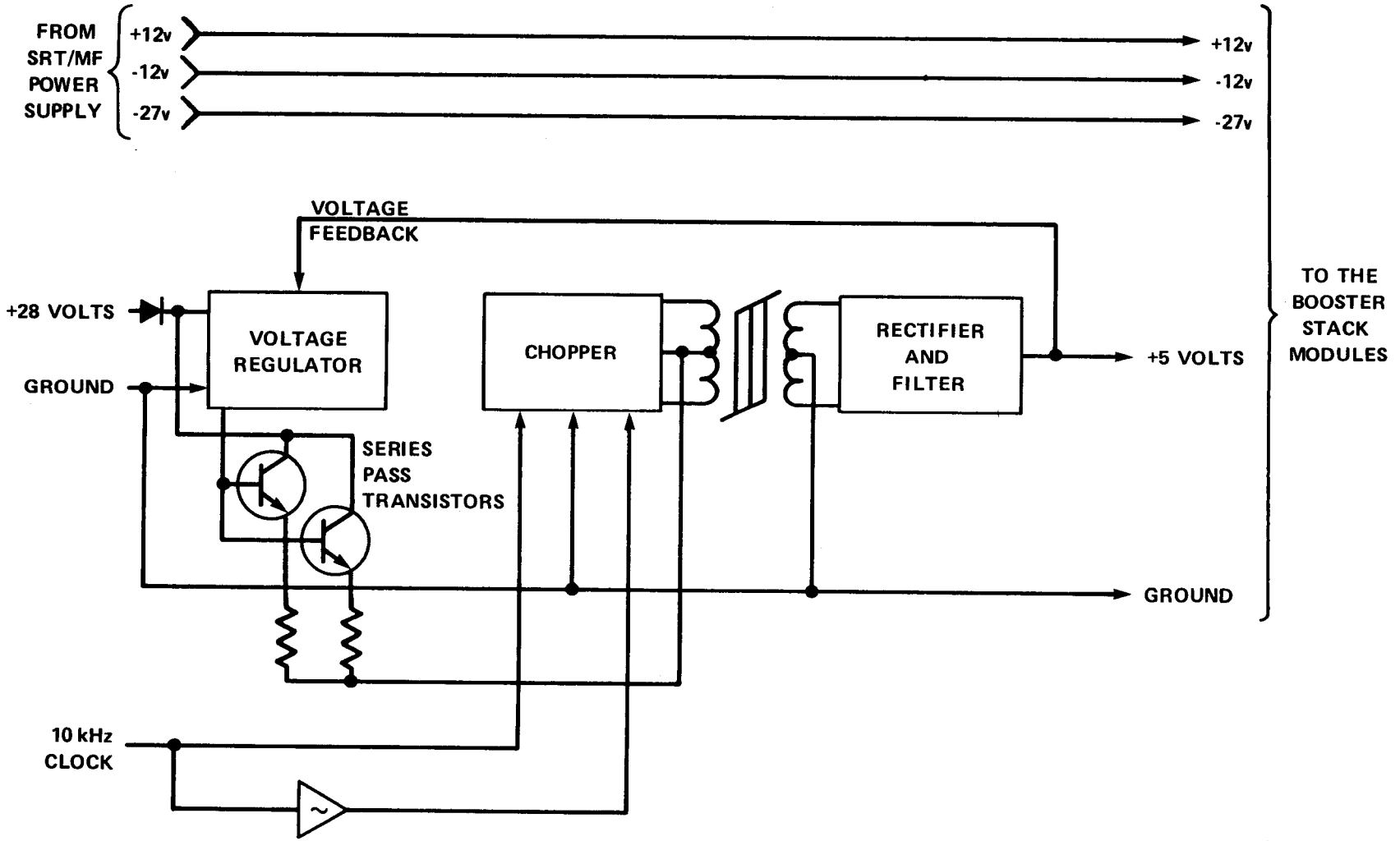


Figure 6.2. BPS-5 Block Diagram

7.0 Packaging

The SRT/MF and all associated modules use AUGAT through-pins for board-to-board connections. As can be seen from the various photos in this book, the modules are open top and bottom and have a metal frame (for exact dimensions, see Appendix A) the same size as the SRT/MF. Modules are stacked on top of each other as shown in the frontispiece photo. A functional diagram of a typical stack is shown in Figure 7.0. Limits on stack size are discussed in Section 6.0. Electrical limits referred to in Section 6.0 are based on the following:

1) The SRT/MF has an excess capacity of 6.5 normalized loads.

2) The BPS-5 also has a capacity of 6.5 loads.

3) The modules present the following loads:

Module	Load when on Main Stack	Load to BPS-5 when on Booster Stack	Addition Load to SRT/MF when on Booster Stack
AS-32	1.0	0.25	0.75
ASC-32	1.75	(Never used on Booster Stack)	
RCM-4	1.0	1.0	0
SIDL-8	1.0	1.0	0
SIDL-16	0.5	0.5	0
BUF-4	0.25	0.25	0
PAC-16	2.0	0.50	1.5
TEM	0.1	(Never used on Booster Stack)	
RBM	0	0	0

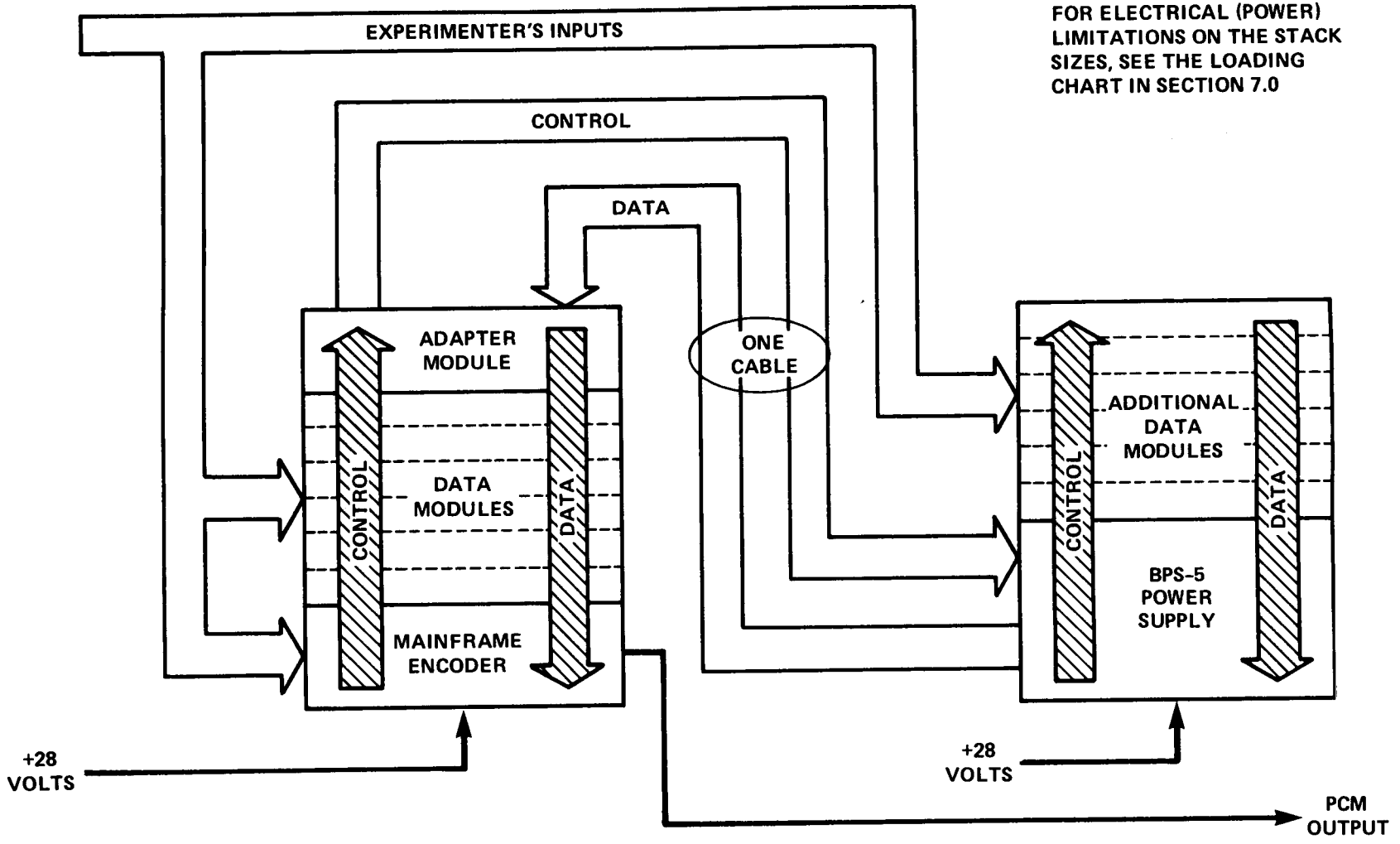
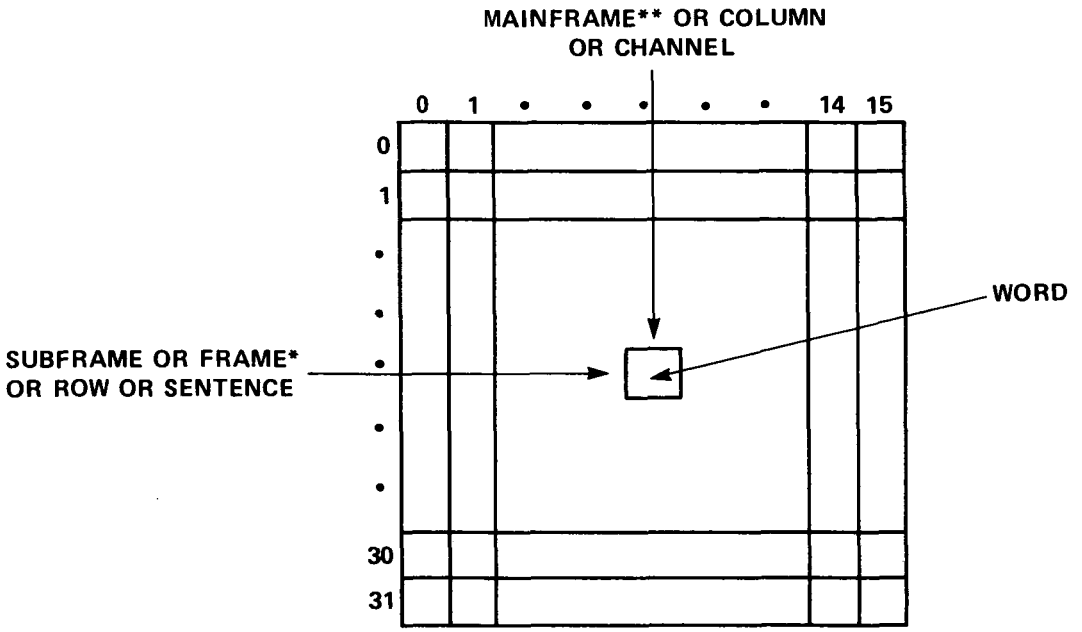


Figure 7.0. Packaging Diagram

8.0 Configuration Terminology

The data format of the PCM system is a matrix with the following terminology:



Specification of a position, or set of positions in the matrix is made by the so-called "C-S-D" code. The "C" is the channel number and the "S" is the subframe number.

The C-S of the C-S-D code can then be used to designate any of the 512 words in the data matrix of Figure 2.0.2. The "D" designator represents a repetition rate of 2^D subframes. That is, for the following values of D, the word designated by the "C-S" portion of the address code repeats at the given subframe rate:

Value of D	Subframe Repetition Rate
0	1 ($=2^0$)
1	2 ($=2^1$)
2	4 ($=2^2$)
3	8 ($=2^3$)
4	16 ($=2^4$)
5	32 ($=2^5$)

*"Frame" is a general term for rows; when discussing a specific row it would normally be referred to as a subframe and by number: The 17th frame is called subframe 16.

**"Mainframe" is a general term for columns; when discussing a specific column it would normally be referred to as a channel and by number: The 11th column is called channel 10.

Let us consider the address 8–3–5. This represents a data word in column #8, row #3, with a repetition rate of $2^5 = 32$ subframes. Adding 32 (the repetition rate) to 3 (the original subframe number), we get 32 + 3 = 35. This means that the data repeats in column 8, row 35. But of course there is no row 35, as the matrix only has 32 rows. Taking 35 modulo 32, we have $(35)_{32} = 3$, and thus 8–3–5 does not repeat until row 3 of the next paragraph. Should the reader be unfamiliar with modular systems, simply look at it as putting a second paragraph below the first and then starting to number the rows of the lower paragraph at 32 rather than 0. The 35th row will be seen to be the one which would have been labeled 3 had the row numbering for the second paragraph started with 0.

So we see that D = 5 implies a unique word in the paragraph; that is, one which does not repeat within the paragraph. This is an important point in the nomenclature and should be kept in mind during the following discussion and, indeed, during any discussion of the data addressing on the sounding rocket PCM system.

Now consider the address 8–3–4. The C = 8 implies column 8, the S = 3 implies row 3, but now D = 4 (rather than 5 as in the previous example) and this implies a repetition at every 16 subframes starting with the one specified by the "C–S" (= 8–3) portion of the address. So, the address 8–3–4 implies a data point at column #8, row #3, and another at column #8, row #19. The second point is arrived at by adding the original subframe # (S = 3) to the repetition rate ($2^4 = 16$) implied by the degree of commutation (D = 4).

The next repetition is at row 19 + 16 = 35 but again we have $[35]_{32} = 3$ so this repetition is simply the original word, but in the next paragraph.

Now consider the following:

$$8\text{–}3\text{–}4 \equiv \{8\text{–}3\text{–}5 \text{ plus } 8\text{–}19\text{–}5\}$$

If the "D" were not used at all, we could just as easily refer to the right side of the above equivalence as "8–3 plus 8–19", but by adding the D to the C–S code, we can now use 8–3–4 in place of "8–3 plus 8–19". This shorthand becomes rather more useful as we consider lower values of D. For example:

$$8\text{–}3\text{–}2 \equiv \left\{\begin{array}{l} 8\text{–}3\text{–}5 \\ \text{plus } 8\text{–}7\text{–}5 \\ \text{plus } 8\text{–}11\text{–}5 \\ \text{plus } 8\text{–}15\text{–}5 \\ \text{plus } 8\text{–}19\text{–}5 \\ \text{plus } 8\text{–}23\text{–}5 \\ \text{plus } 8\text{–}27\text{–}5 \\ \text{plus } 8\text{–}31\text{–}5 \end{array}\right\}$$

By now, the utility of the D portion of the code should be clear. Since the D designator is a shorthand notation, it is sometimes left off. Any notation of the form "C–S", implies a D = 5. Thus 8–3 implies 8–3–5. It should also be noted that

$$8\text{–}X\text{–}0 \equiv \text{channel 8}$$

and that this is true regardless of the value of "X". Thus, for example:

$$8\text{–}3\text{–}0 \equiv 8\text{–}16\text{–}0 \equiv \text{channel 8}$$

Although the "D" portion of the address code allows any level of subcommutation to be described, it cannot handle supercommutation of mainframes. For example how does one describe the fact that channels 2 and 10 are used for the same data point? The nomenclature used is this:

2, 10–0–0, thus "C" = 2, 10 thereby describing multiple channels.

Figure 8.0.1 (2 sheets) shows a signal allocation arrived at jointly by both the experimenter and by code 743.4. The columns labeled "Signal Name" and "Samples per Second" are filled out by the experimenter and the column labeled "Program Designation" is filled out by Code 743.4. It is possible, if circumstances necessitate it, for the experimenter to do some or all of the "Program Designation", but in general:

> Experimenters please note: the "Program Designation" is to be assigned by Code 743.4, not by the experimenter.

The mnemonics in Figure 8.0.1 are based on the following:

S = serial data (SIDL–16)

A = analog data (AS–32, ASC–32)

C = count data (RCM–4)

E = event monitors (ASC–32)

P = parallel digital (RBM–4)

F = Fifo Data (FIFO–2)

T = time–even monitor data (TEM–4)

CAL = Internal Calibration Data

Figure 8.0.2 (2 sheets) shows the identical information but organized by channel # order. Figure 8.0.3 shows the same information again (except for comments) organized into a data matrix. It might be useful for the reader to examine the relationship between the C–S–D codes of Figures 8.0.1 and 8.0.2 with the data matrix position of Figure 8.0.3 for the same signals.

Signal Name	Program Designation	Samples Per Second	Comments
S1	2, 10-0-0	2500	supercommutated
S2	3, 11-0-0	2500	supercommutated
S3	15-4-3	160	
D1	15-0-5	40	9 bit parallel binary input
CAL	15-31-5	40	internal calibrator (5V, 4V, 3V, 2V, 1V, 0V, 0V, 0V)
C1	5-0-3	160	
C2	5-1-3	160	
C3	5-2-3	160	
C4	5-3-3	160	
C5	5-4-3	160	
C6	5-5-3	160	
C7	5-6-3	160	
C8	5-7-3	160	
C9	5-0-2	320	
C10	6-1-2	320	
C11	6-2-2	320	
C12	6-3-2	320	
C13	7-0-1	640	
C14	7-1-1	640	
C15	15-2-5	40	
C16	15-18-5	40	
A1	4, 12-0-0	2500	
A2	8-0-2	320	
A3	8-1-2	320	
A4	8-2-3	160	
A5	8-6-3	160	
A6	8-3-5	40	
A7	8-7-5	40	
A8	8-11-5	40	
A9	8-15-5	40	
A10	8-19-5	40	
A11	8-23-5	40	
A12	8-27-5	40	

Figure 8.0.1. Signal Allocation Table (Page 1 of 2)

Signal Name	Program Designation	Samples Per Second	Comments
A13	8-31-5	40	
A14	9-0-5	40	
↓	↓	↓	
A45	9-31-5	40	
A46	13-0-0	1250	
A47	14-0-4	80	
A48	14-1-4	80	
A49	14-2-4	80	
A50	14-3-5	40	
↓	↓	↓	
A62	14-15-5	40	
A63	14-19-5	40	
↓	↓	↓	
A75	14-31-5	40	
A76	15-1-5	40	
A77	15-3-5	40	
A78	15-5-5	40	NOTE: In an actual allocation table, this column would be filled in with comments
A79	15-6-5	40	
A80	15-7-5	40	
A81	15-8-5	40	
A82	15-9-5	40	
A83	15-10-5	40	
A84	15-11-5	40	
A85	15-13-5	40	
A86	15-14-5	40	
A87	15-15-5	40	
A88	15-16-5	40	
A89	15-17-5	40	
A90	15-19-5	40	
A91	15-21-5	40	
A92	15-22-5	40	
A93	15-23-5	40	
A94	15-24-5	40	
A95	15-25-5	40	
A96	15-26-5	40	
A97	15-23-5	40	
A98	15-29-5	40	
A99	15-30-5	40	

Figure 8.0.1. Signal Allocation Table (Page 2 of 2)

Channel	Signal Name	Description and/or Comments
0-0-0	sync	
1-0-0	sync & subframe count	
2-0-0	S1	(supercommutated with 10-0-0)
3-0-0	S2	(supercommutated with 11-0-0)
4-0-0	A1	(supercommutated with 12-0-0)
5-0-3	C1	
5-1-3	C2	
5-2-3	C3	
5-3-3	C4	
5-4-3	C5	
5-5-3	C6	
5-6-3	C7	
5-7-3	C8	
6-0-2	C9	
6-1-2	C10	
6-2-2	C11	NOTE: In an actual channel allocation chart, this column would be full of comments
6-3-2	C12	
7-0-1	C13	
7-1-1	C14	
8-0-2	A2	
8-1-2	A3	
8-2-3	A4	
8-6-3	A5	
8-3-5	A6	
8-7-5	A7	
8-14-5	A8	
8-15-5	A9	
8-19-5	A10	
8-23-5	A11	
8-27-5	A12	
8-31-5	A13	
9-0-5	A14	
9-1-5	A15	
↓	↓	
9-31-5	A45	

Figure 8.0.2. Channel Allocation Table (Page 1 of 2)

Channel	Signal Name	Description and/or Comments
10-0-0	See 2-0-0	
11-0-0	See 3-0-0	
12-0-0	See 4-0-0	
13-0-0	A46	
14-0-4	A47	
14-1-4	A48	
14-2-4	A49	
14-3-5	A50	
14-4-5	A51	
↓	↓	
14-15-5	A62	
14-19-5	A63	
14-20-5	A64	
↓	↓	
14-31-5	A75	
15-0-5	D1	(9 bit parallel binary)
15-1-5	A76	
15-2-5	C15	
15-3-5	A77	
15-4-3	S3	
15-5-5	A78	
15-6-5	A79	
↓	↓	
15-11-5	A84	
15-13-5	A85	
15-14-5	A86	
15-15-5	A87	
15-16-5	A88	
15-17-5	A89	
15-18-5	C16	
15-19-5	A90	
15-21-5	A91	
15-22-5	A92	
15-23-5	A93	
15-24-5	A94	
15-25-5	A95	
15-26-5	A96	
15-27-5	A97	
15-29-5	A99	
15-30-5	A99	
15-31-5	CAL	(internal calibrator)

Figure 8.0.2. Channel Allocation Table (Page 2 of 2)

Mainframe Channel Number																
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
↑	↑	S1	S2	A1	C1	C9	C13	A2	A14	S1	S2	A1	A46	A47	D1	0
		S1	S2	A1	C2	C10	C14	A3	A15	S1	S2	A1	A46	A48	A76	1
		S1	S2	A1	C3	C11	C13	A4	A16	S1	S2	A1	A46	A49	C15	2
		S1	S2	A1	C4	C12	C14	A6	A17	S1	S2	A1	A46	A50	A77	3
		S1	S2	A1	C5	C9	C13	A2	A18	S1	S2	A1	A46	A51	S3	4
		S2	S2	A1	C6	C10	C14	A3	A19	S1	S2	A1	A46	A52	A78	5
		S1	S2	A1	C7	C11	C13	A5	A20	S1	S2	A1	A46	A53	A79	6
		S1	S2	A1	C8	C12	C14	A7	A21	S1	S2	A1	A46	A54	A80	7
		S1	S2	A1	C1	C9	C13	A2	A22	S1	S2	A1	A46	A55	S81	8
		S1	S2	A1	C2	C10	C14	A3	A23	S1	S2	A1	A46	A56	A82	9
		S1	S2	A1	C3	C11	C13	A4	A24	S1	S2	A1	A46	A57	A83	10
		S1	S2	A1	C4	C12	C14	A8	A25	S1	S2	A1	A46	A58	A84	11
		S1	S2	A1	C5	C9	C13	A2	A26	S1	S2	A1	A46	A59	S3	12
		S1	S2	A1	C6	C10	C14	A3	A27	S1	S2	A1	A46	A60	A85	13
Allocated For Sync Sub Frame Counter		S1	S2	A1	C7	C11	C13	A5	A28	S1	S2	A1	A46	A61	A86	14
		S1	S2	A1	C8	C12	C14	A9	A29	S1	S2	A1	A46	A62	A87	15
		S1	S2	A1	C1	C9	C13	A2	A30	S1	S2	A1	A46	A47	A88	16
		S1	S2	A1	C2	C10	C14	A3	A31	S1	S2	A1	A46	A48	A89	17
		S1	S2	A1	C3	C11	C13	A4	A32	S1	S2	A1	A46	A49	C16	18
		S1	S2	A1	C4	C12	C14	A10	A33	S1	S2	A1	A46	A63	A90	19
		S1	S2	A1	C5	C9	C13	A2	A34	S1	S2	A1	A46	A64	S3	20
		S1	S2	A1	C6	C10	C14	A3	A35	S1	S2	A1	A46	A65	A91	21
		S1	S2	A1	C7	C11	C13	A5	A36	S1	S2	A1	A46	A66	A92	22
		S1	S2	A1	C8	C12	C14	A11	A37	S1	S2	A1	A46	A67	A93	23
		S1	S2	A1	C1	C9	C13	A2	A38	S1	S2	A1	A46	A68	A94	24
		S1	S2	A1	C2	C10	C14	A3	A39	S1	S2	A1	A46	A69	A95	25
		S1	S2	A1	C3	C11	C13	A4	A40	S1	S2	A1	A46	A70	A96	26
		S1	S2	A1	C9	C12	C14	A12	A41	S1	S2	A1	A46	A71	A97	27
		S1	S2	A1	C5	C9	C13	A2	A42	S1	S2	A1	A46	A72	S3	28
		S1	S2	A1	C6	C10	C14	A3	A43	S1	S2	A1	A46	A73	A98	29
		S1	S2	A1	C7	C11	C13	A5	A44	S1	S2	A1	A46	A74	A99	30
↓	↓	S1	S2	A1	C8	C12	C14	A13	A45	S1	S2	A1	A46	A75	CAL	31

Sub Frame No's.

Figure 8.0.3. Sample Data Matrix

9.0 A Summary of Ground Support Capabilities

For those experimenters who have not previously used the system, a brief summary is given here of ground station capabilities associated with the PCM system.

Permanent Flight Recording: The ground station operators will make one or more video tapes for each TM system of a flight. This tape is the permanent property of NASA/GSFC. Experimenters may obtain a dub of the tape but that should not be necessary except in rare cases. During payload integration, a tape can be made but will be saved only for a few days (longer if absolutely necessary).

Front Panel Display: The PCM decommutator has a digital readout and a binary readout for the same single channel of data. Channel selection is by thumb-wheel switch and can only be selected in the form C-S-0 or C-S-5. There are two decoms per station, so two signals can be monitored.

CRT Bar-Graph: The ground station includes a CRT bar-graph which gives a fixed format representation of the entire data matrix in the form of 16 vertical bars, which show the data on each of the 16 main channels. It should be noted that channels with many different signals in the subchannels cannot be seen very clearly via the bar graph, although the bar graph is quite useful for monitoring full-time channels. There are two CRT's per station.

CRT Strip-Chart: The ground station CRT can be switched from bar-graph to an alternate mode during which it acts as a 256-data-point window of approximately 10 centimeters physical length.

The data selection is by thumb wheel switch and must be of the form C-S-0 or C-S-5. The CRT displays a strip-chart-like graph of the last 256 data points. For a 200kHz system, with a C-S-5 selection, the 10cm display shows approximately 6.4 seconds of data. For a C-5-0 selection, the display shows the last .2 seconds of data. In either case, the display can be locked at any point so that particular data areas can be examined in detail while not moving. This CRT-strip chart display is most useful during payload integration when it is not yet necessary to have a hard copy strip chart.

Strip Chart: The ground station has two electrostatic strip chart recorders. Paper speed can be selected from 1/8 in/sec to 2 in/sec. Channel width is a function of the number of channels to be plotted, as follows:

Number of Channels to be Plotted	Size of Plot per Channel	Number of Bits in Plot per Channel
1	5"	512
2→3	2.5"	256
4→7	1.25"	128
8→15	0.625"	64

This scaling is hardwired automatic and cannot be changed to give one scale for one channel and a different scale for another channel in the same plot.

Paper for the strip chart is available in either roll or Z-fold. The Z-fold paper has the advantage of being "random access" in the sense that any portion of the plot can be accessed with the same speed as any other portion. Rools, of course, must be rolled up to get from one portion to another. The Z-fold has a slight tendancy to drop a few points out of the plot at each edge where the paper folds, so that Z-fold is most useful during integration, but the experimenter may desire to use roll paper for his final flight strip-charts.

Back-of-Chassis Plug: Every ground station has a plug on the back which can be used by the experimenter for his own GSE. The plug is described in detail in Appendix D of this document.

Computer: The ground stations at GSFC and WSMR have a computer system. One portable computer system is available for field use. Experimenters requiring direct computer support during flight should request assignment of the portable system (if not flying from WSMR) as soon as possible. The computer provides the following services:

"FORMAT" Computer Tape: A standard-format tape (described fully in Appendix E of this document) can be provided for every TM system of every flight whether or not there is a computer at the launch site. The experimenter is expected to use this tape for most of his post-flight data reduction. It is the experimenters responsibility to request this tape. See Appendix E for request form.

"PLOT" Computer-Strip-Chart: This is a strip chart almost identical in format to the one provided by the ground station. The main differences are speed (only 1", 2" and 4"/sec) and size; 1 channel = 14" rather than 5", and subsequent scaling is proportionally larger. Also, the maximum number of channels is 12 rather than 15.

"FPLOT" Computer Strip Chart: This is a strip chart which can be made only by the computer from the tape generated by the "FORMAT" program. It is similar to the previously mentioned strip charts but, again, has different speeds (.391, .781, 1.56, 3.12, 6.25 and 12.5 in/sec). Plot size is identical to that for the "PLOT" strip chart (14" for 1 channel, etc.). This chart has the additional feature that there will be a 1-sec time grid and an accompanying printed time code on the chart.

> The experimenter is warned that this is not a real time plot and that to plot one minute of data takes typically 5 minutes. Only short runs should be requested.

"LIST" Computer Printout: This is a digital (numeric, decimal) listing of every data value in every paragraph between specified time intervals.

> Experimenters are warned that this is not a real-time listing, and that to list one second of data takes about 10 minutes: Only very short runs should be requested.

"DCOM" Computer Listing: This is a listing of selected data values between given time intervals. While not real time, it is much faster than "LIST".

General Comments About the Computer: The computer is available for special use by the experimenter if he so desires. Several documents are being prepared relating to the computer system. Inquiries should be directed to Mr. Raymond Stattel (301-982-5304).

APPENDIX A

SUMMARY OF SPECIFICATIONS

APPENDIX A

SUMMARY OF SPECIFICATIONS

1. Mainframe Encoder

Output Bit Rate:	200 kilobits/second (50kb also available)
Word Rate:	20 kilowords/second (MSB first, parity last)
Mainframe:	2 sync words plus 14 data words
Subframe:	32 subframes per mainframe
Parity:	Odd
Word:	9 data bits plus parity bit
Output Code:	Bi-Ø-L
Output Voltage:	"1" = positive transition, "0" = negative transition
Analog Input Voltage Range:	-0.1 to +5.1 volts
Analog Input Protection:	To ±30 volts
Analog Input DC Impedance:	1 megohm
Analog Input Maximum Source Impedance:	5.6 kilohm
Power Input:	+26 to +34 volts DC @ 300 milliamperes (9 watts)
Power Efficiency:	70% @ 32 volt, full load
Residual Power: (For expansion modules)*	+5 volt @ 1.3 amps (6.5 watts) +12 volt @ 250ma (3 watts) -12 volt @ 250ma (3 watts) -27 volt @ 250ma (6.75 watts)
Length:	9.5 centimeter
Width:	9.5 centimeter
Height:	5.5 centimeter
Weight:	595 grams

2. Programmable Address Counter (PAC-16)

Memory Size:	512 words x 8 bits
Power Input:	+5 volt @ 60ma, -12 volt @ 120ma
Height:	1.3 centimeter
Weight:	130 grams

*Total dissipation not to exceed 6.5 watts.

3. Analog Submultiplexer (AS-32)

Analog Inputs:	32 channels
Analog Input Voltage Range:	-0.1 to +5.1 volts
Analog Input Protection:	To ±30 volts
Analog Input DC Impedance:	1 megohm
Analog Input Maximum Source Impedance:	5.6 kilohms (See Appendix C)
Power Input:	+5 volt @ 80ma, -27 volt @ 25ma
Height:	0.65 centimeter
Weight:	89 grams

4. Analog Submultiplexer with Calibration and Bi-Level Monitor (ASC-32)

Digital Inputs:	9 bits
Digital Input Logic:	TTL ("0" = 0 volts @ -0.8ma, "1" = +5 volts @ 0.025ma
Calibration Levels:	0, 1, 2, 3, 4 and 5 volts
Analog Inputs:	30 channels
Analog Input Voltage Range:	-0.1 to +5.1 volts
Analog Input Protection:	To ±30 volts
Analog Input DC Impedance:	1 megohm
Analog Input Maximum Source Impedance:	5.6 kilohms (See Appendix C)
Power Input:	+5 volt @ 100ma +12 volt @ 5ma -12 volt @ 5ma -27 volt @ 35ma
Height:	1.3cm
Weight:	182 grams

5. Counter Module (RCM-4)

Count Inputs:	4 channels (each to a 9-bit accumulator)
Count Input Logic:	Low power TTL (1 unit load)
Power Input:	+5 volt @ 200ma
Height:	0.65cm
Weight:	93 grams

6. Serial Input Data Loader (SIDL-8)

Serial Inputs:	Four 9-bit channels
Serial Input Logic:	TTL (2 unit loads)
Channel Gate and Clock Output Logic:	TTL (10 unit loads)

Power Input:	+5 volt @ 200ma
Height:	0.65 centimeter
Weight:	86 grams

7. Serial Input Data Loader (SIDL-16)

Serial Inputs:	Sixteen 9-bit channels
Serial Input Logic:	TTL (1 unit load)
Enable, Gate, and Clock Outputs:	TTL (10 unit loads)
Power Input:	+5 volt @ 80ma
Height:	0.65 centimeter
Weight:	90 grams

8. Signal Buffer (BUF-4)

Output Logic:	TTL (10 unit loads)
Buffer Input Logic:	TTL (1 unit load)
Power Input:	+5 volt @ 45ma
Height:	0.65 centimeter
Weight:	73 grams

9. Time Event Monitor (TEM-4)

Pulse Inputs:	4 channels
Pulse Input Logic:	TTL (1 unit load)
Power Input:	+5 volt @ 15ma
Height:	0.65 centimeter
Weight:	86 grams

10. Remote Bi-Level Monitor (RBM-4)

Digital Inputs:	Four 9-bit parallel
Digital Input Logic:	TTL ("0" = 0 volts @ -0.8ma, "1" = +5 volts @ 0.025ma)
Power Input:	+26 to +34 volts DC @ 100ma
Inhibit Output Logic:	TTL (10 unit loads)
Size:	8.26cm. L x 7.62cm. W x 2.54cm. H
Weight:	140 grams

11. Booster Power Supply (BPS-5)

Power Input:	+24 to +38Vdc @ 105 milliamperes (nominal)
Power Efficiency:	65% @ 32Vdc, full load
Power Output:	+5Vdc @ 1.25 amperes
Height:	3.6 centimeter
Weight:	524 grams

APPENDIX B

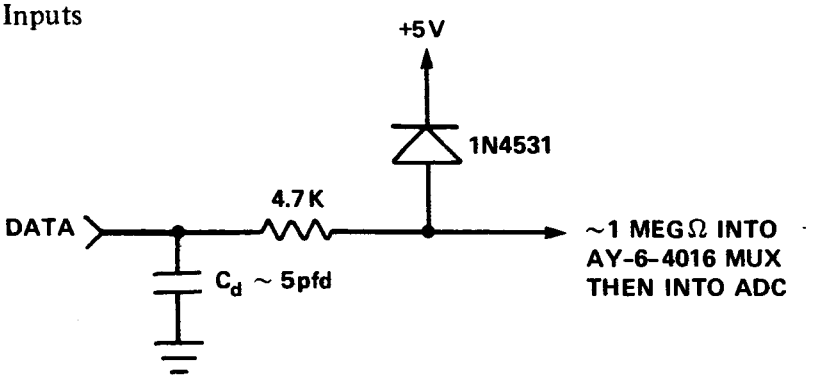
SUMMARY OF EXPERIMENTER INTERFACING

APPENDIX B

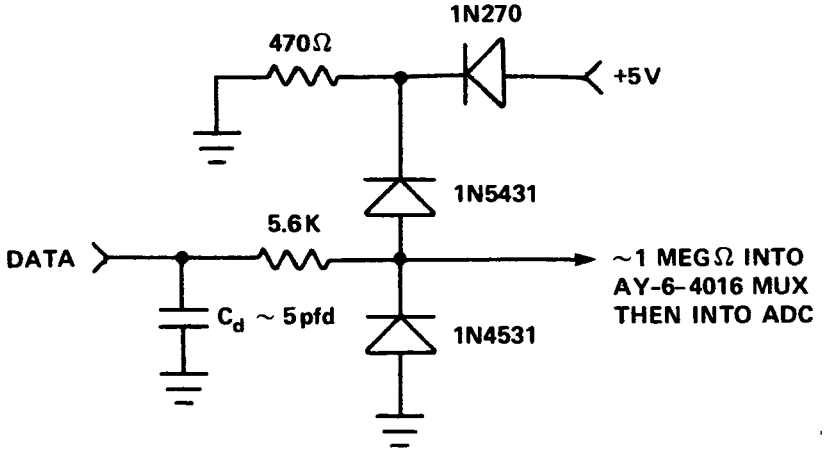
SUMMARY OF EXPERIMENTER INTERFACING

This section gives the precise electrical characteristics of every signal to or from a PCM airborne stack with which an experimenter might need to interface.

Mainframe Analog Inputs

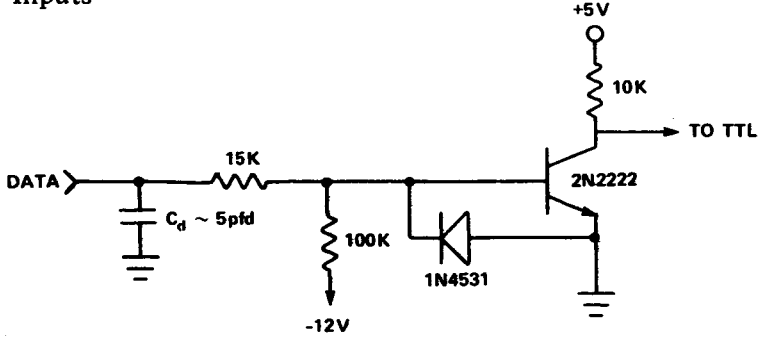


AS-32 Analog Inputs

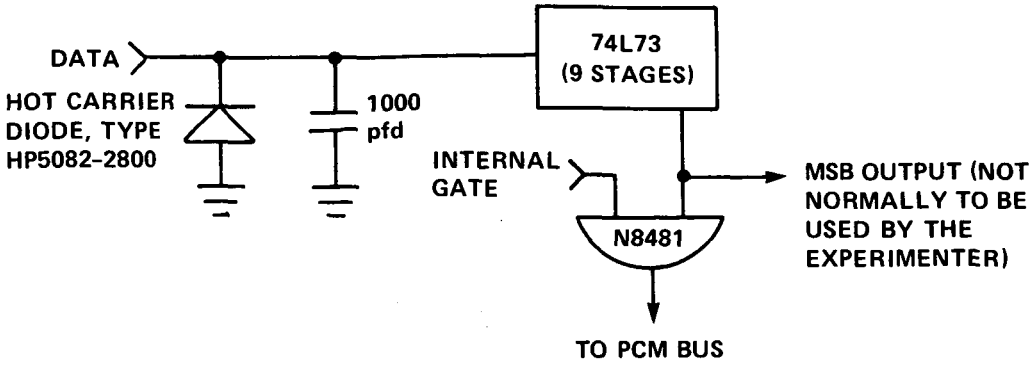


ASC-32 Analog Inputs (identical to AS-32 analog inputs)

ASC-32 Bit Monitor Inputs



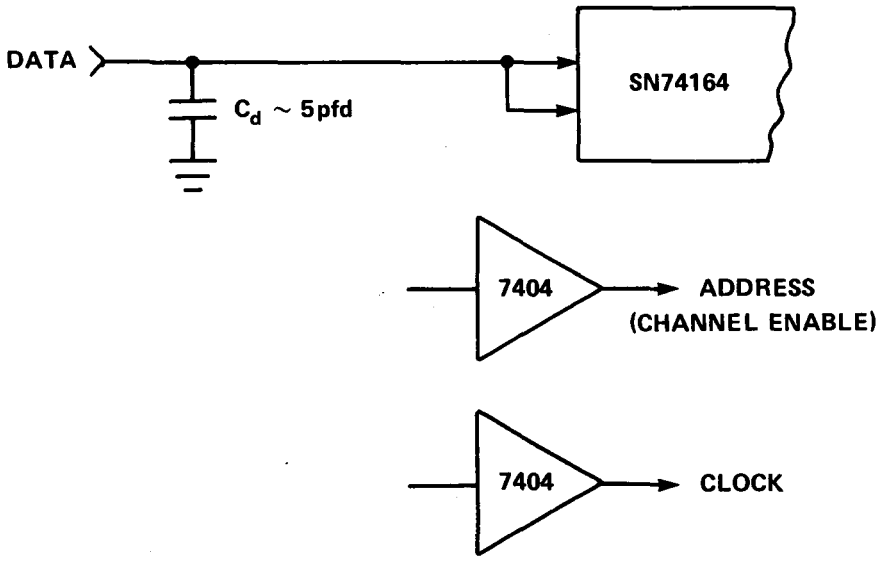
RCM-4 Count Input & MSB Output



maximum frequency: 3.5MHz
minimum pulse width: 150nsec high, 150nsec low

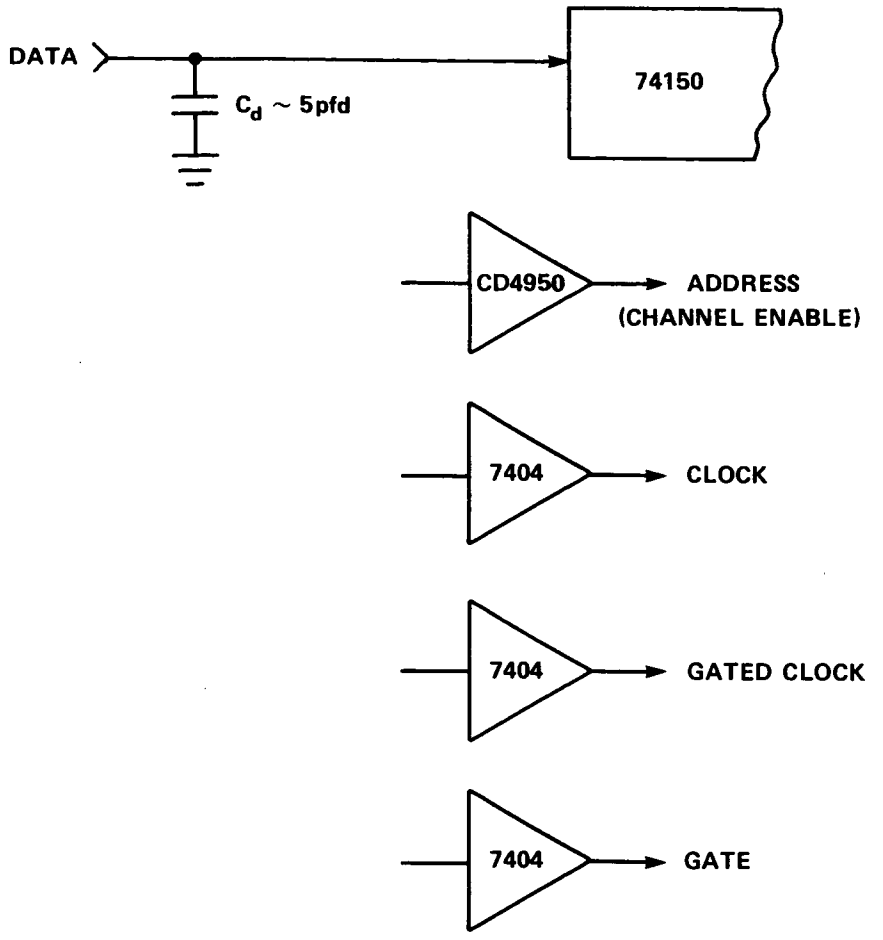
SIDL-8 All Signals

The SIDL-8 is best interfaced to using the circuit shown in Figure B.1. It is crucial to note that the address (channel enable) signal must not be used to edge trigger anything, since it may contain 50nsec spikes at various word boundaries.



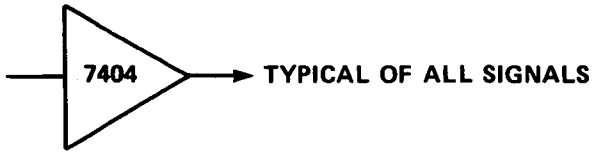
SIDL-16 All Signals

The SIDL-16 is best interfaced to using the circuit shown in Figure B.2. It is crucial to note that the address (channel enable) signal must not be used to edge trigger anything, since it may contain 50nsec spikes at various word boundaries.

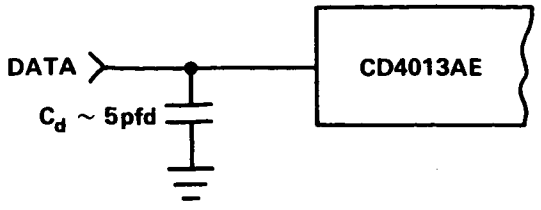


BUF-4 All Signals

All signals from the BUF-4 come from 7404's.

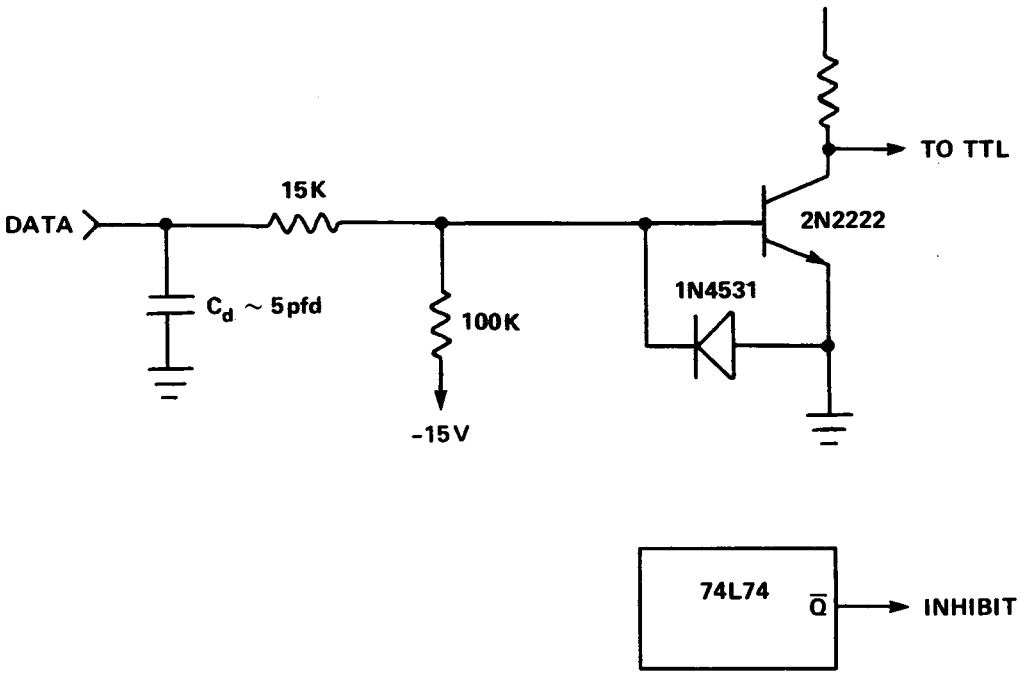


TEM-4 Pulse Inputs



minimum pulse width: 500nsec
maximum pulse frequency: 4MHz
maximum rise and fall times: 15μsec

RBM-4 Digital Input & Inhibit Output



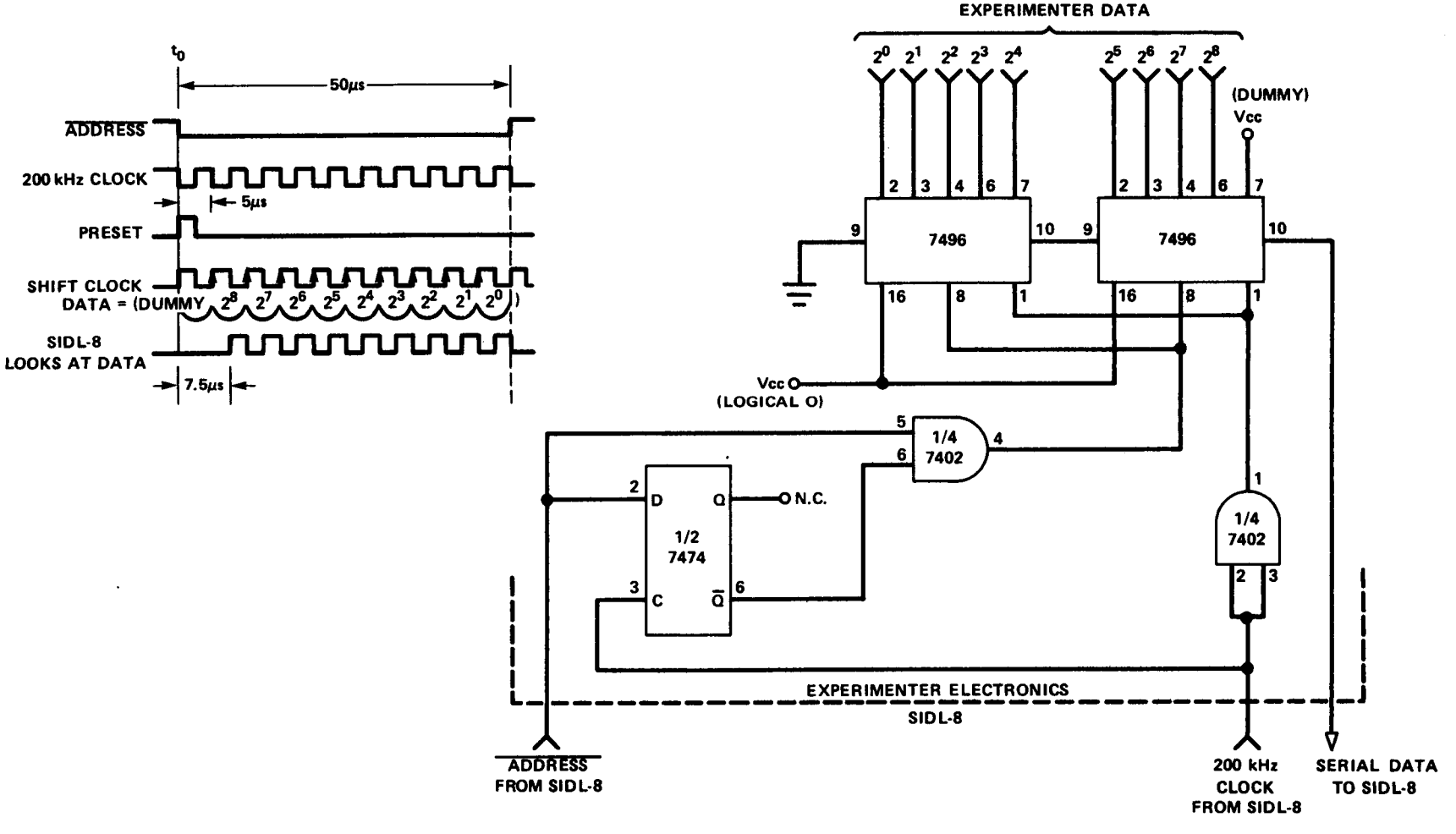


Figure B.1. SIDL–8 Interface

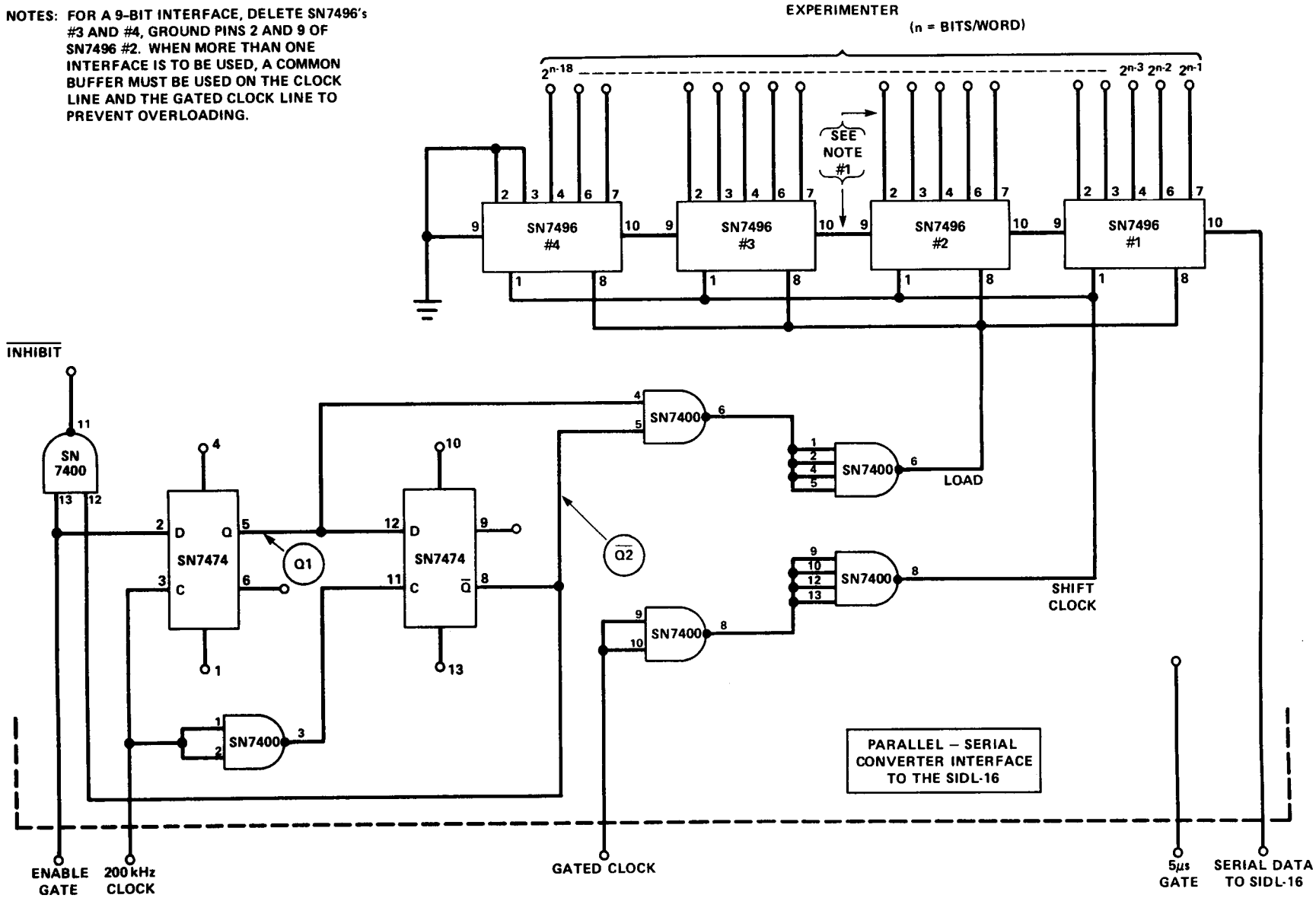


Figure B.2. SIDL–16 Interface

APPENDIX C

DATA MODULE PIN ASSIGNMENT

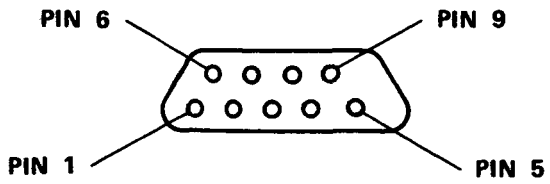


Figure C.1. 9-Pin Microdot Connector

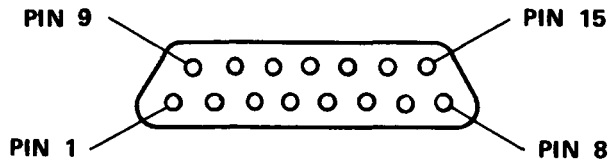


Figure C.2. 15-Pin Microdot Connector

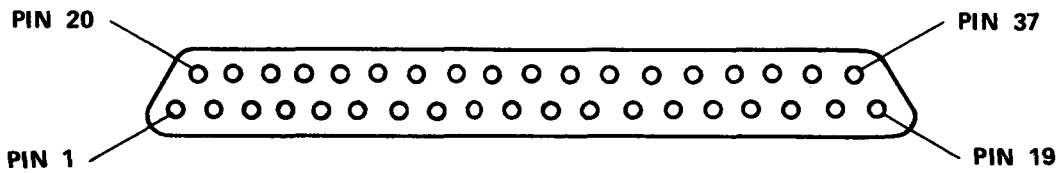


Figure C.3. 37-Pin Microdot Connector

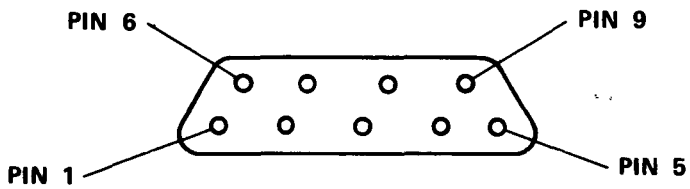


Figure C.4. 9-Pin Cannon Connector

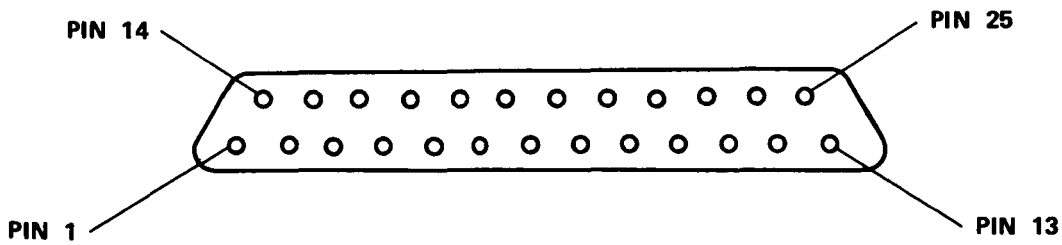


Figure C.5. 25-Pin Cannon Connector

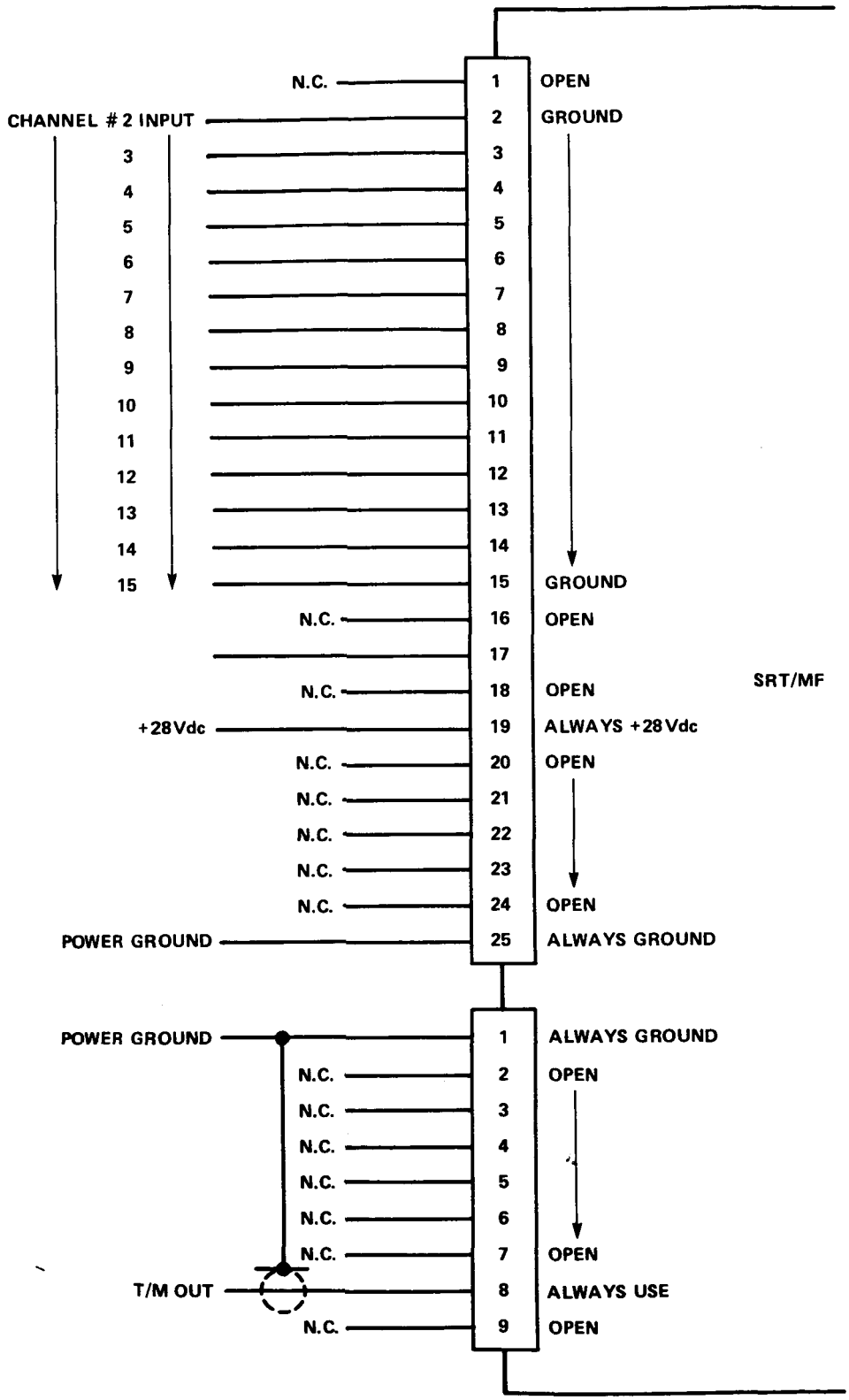


Figure C.6. SRT/MF Pin Assignments

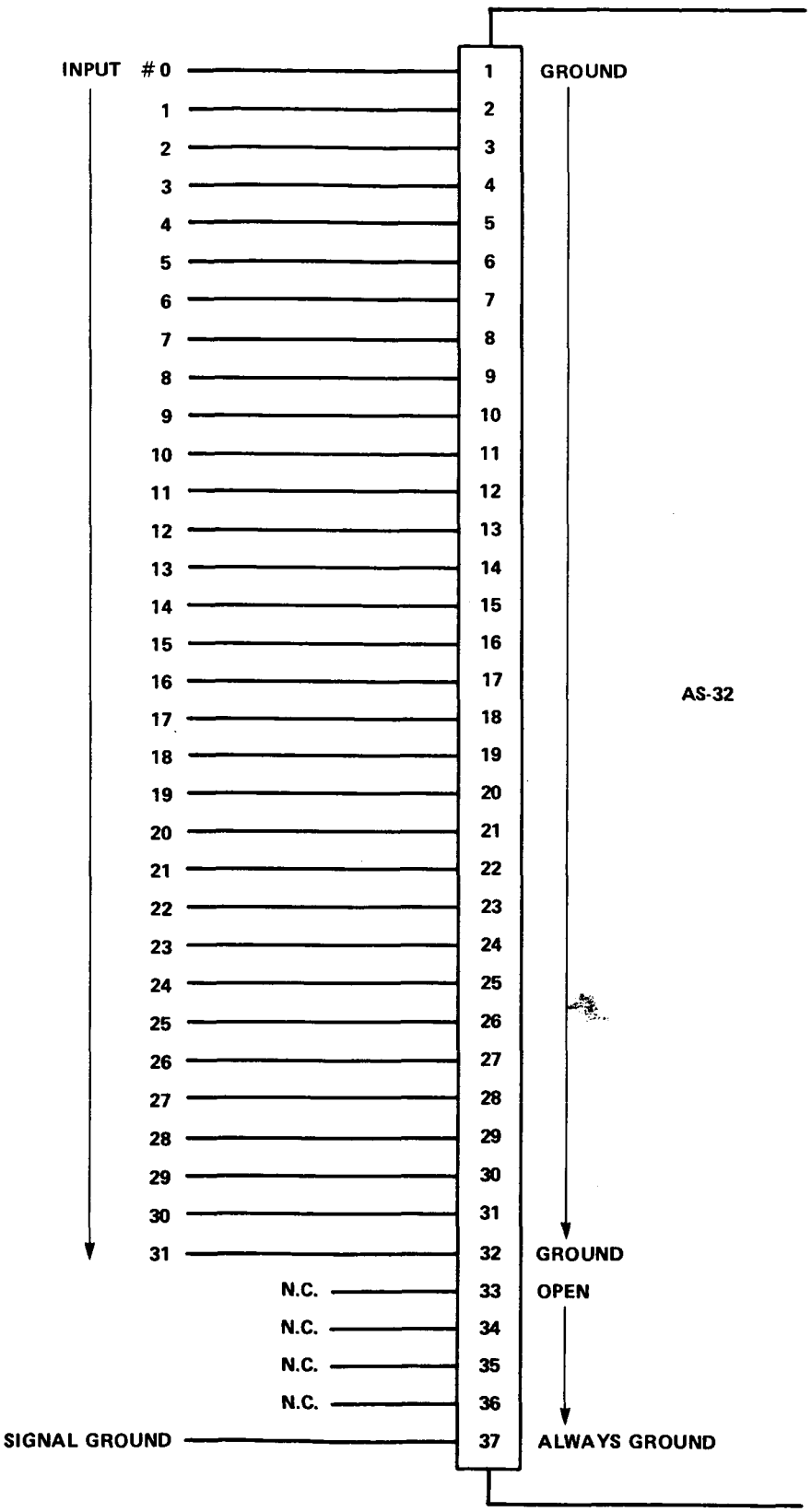


Figure C.7. AS-32 Pin Assignments

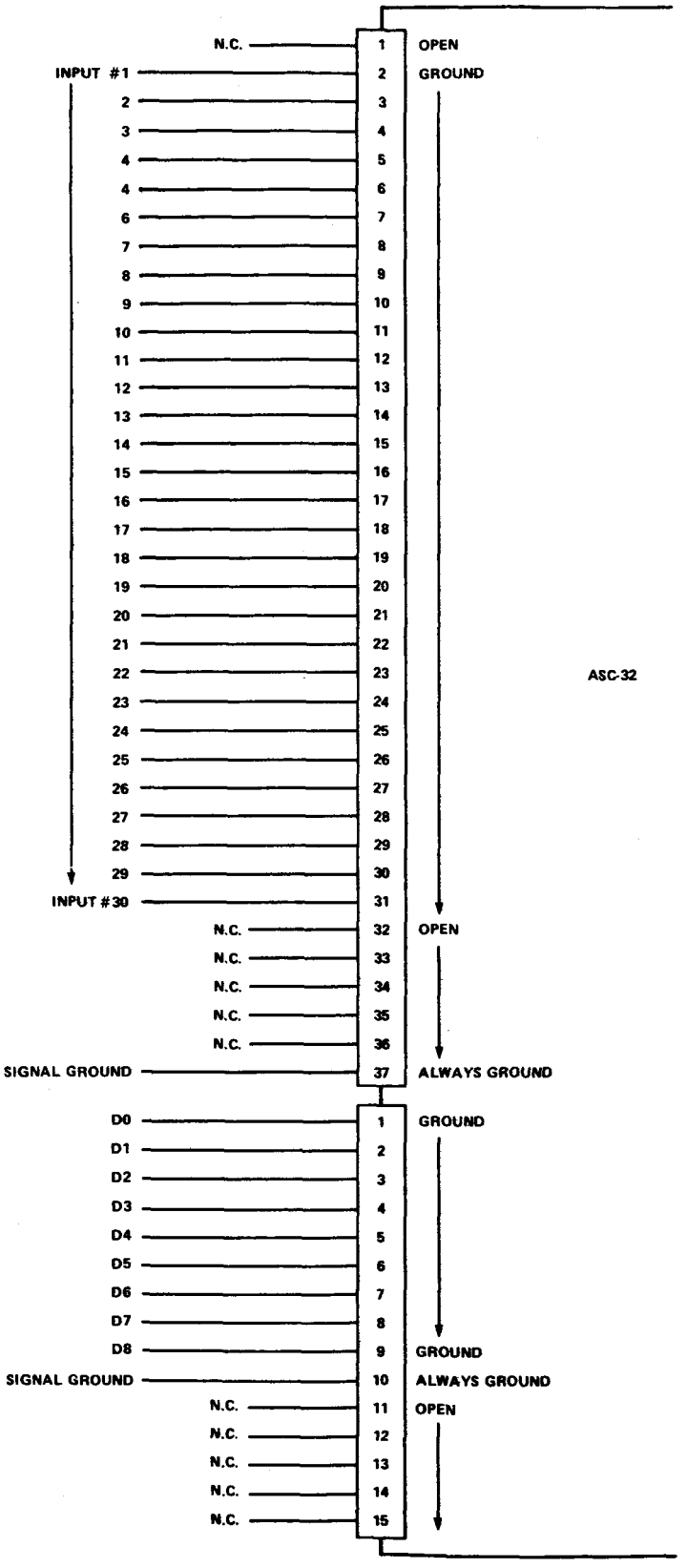


Figure C.8. ASC-32 Pin Assignments

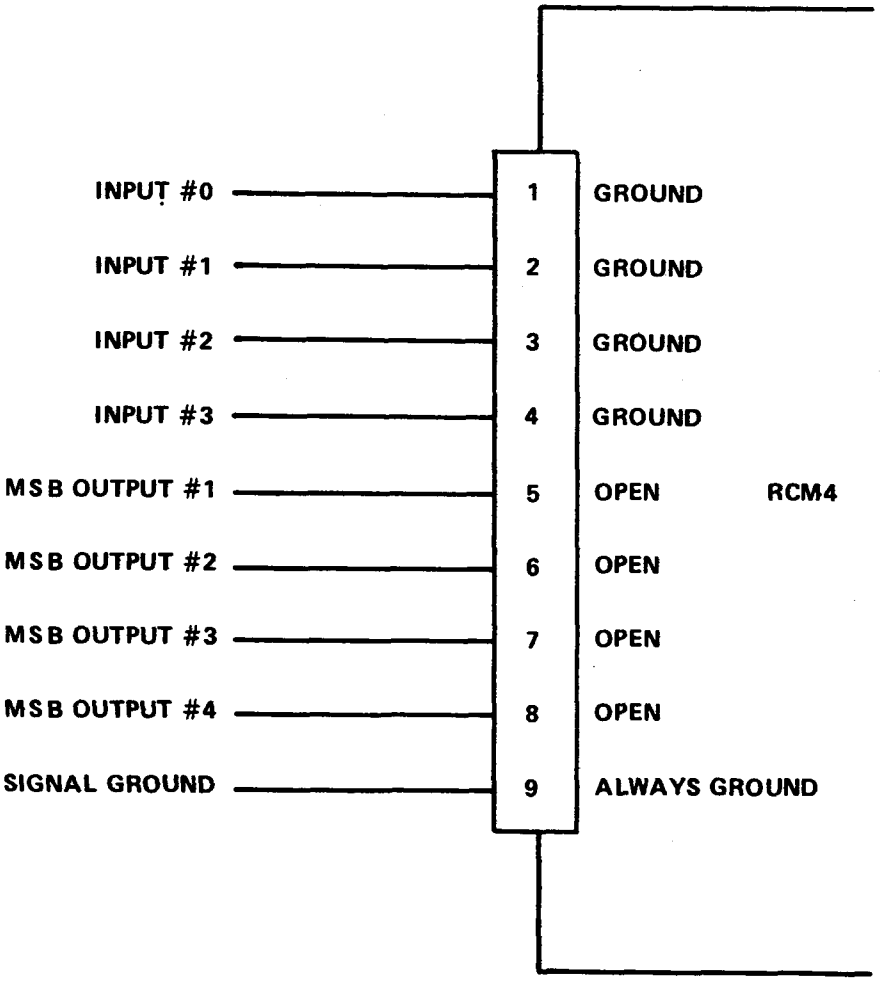


Figure C.9. RCM–4 Pin Assignments

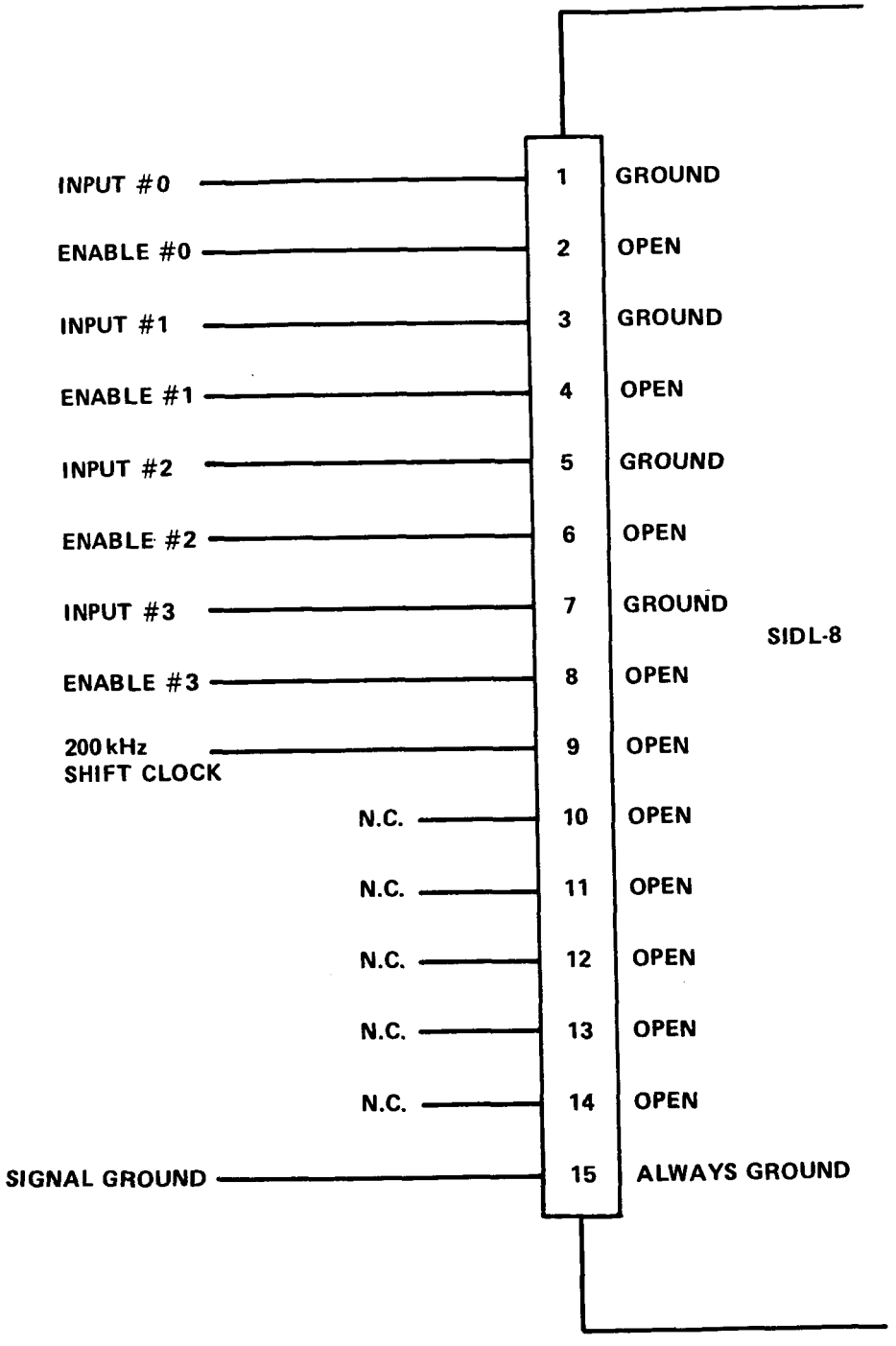


Figure C.10. SIDL-8 Pin Assignments

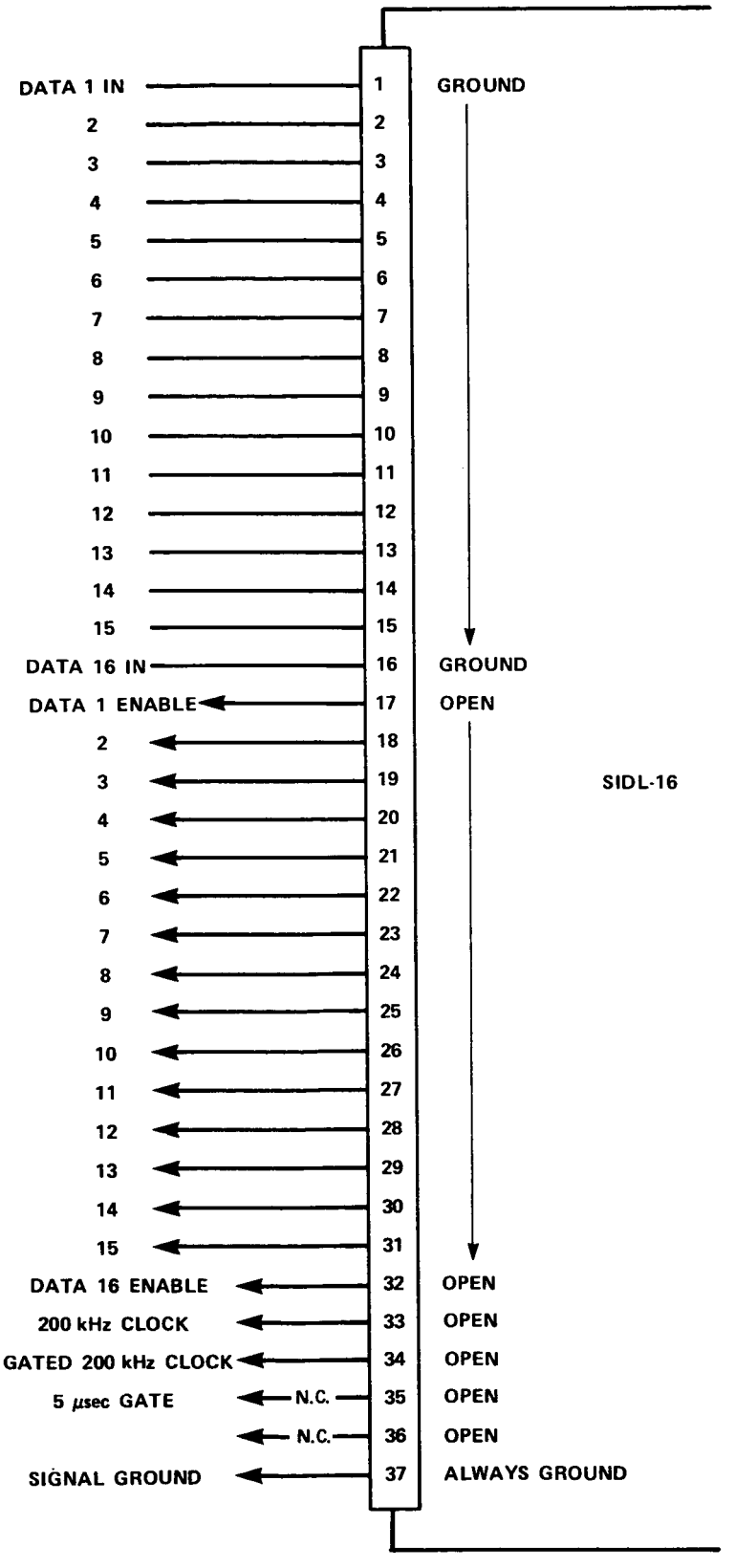


Figure C.11. SIDL-16 Pin Assignments

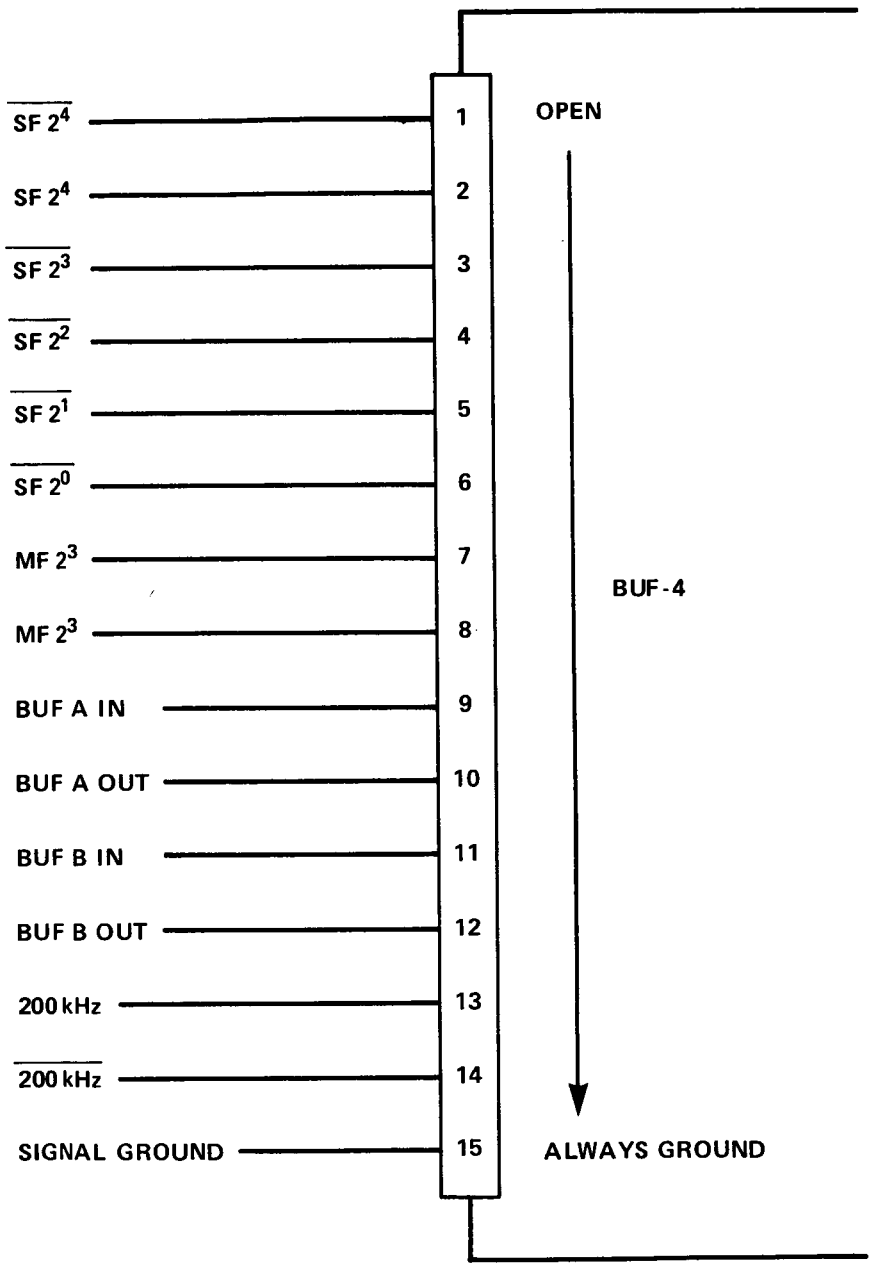


Figure C.12. BUF-4 Pin Assignments

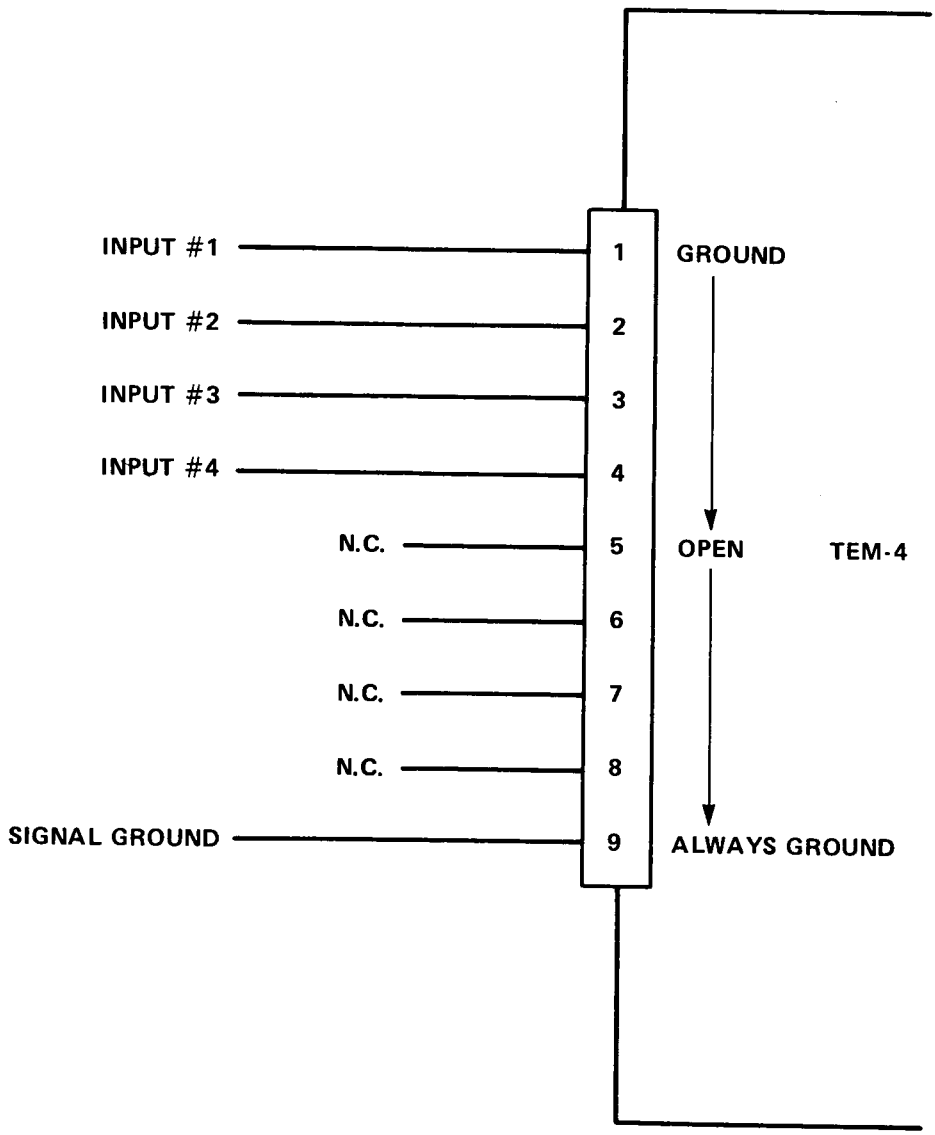


Figure C.13. TEM–4 Pin Assignments

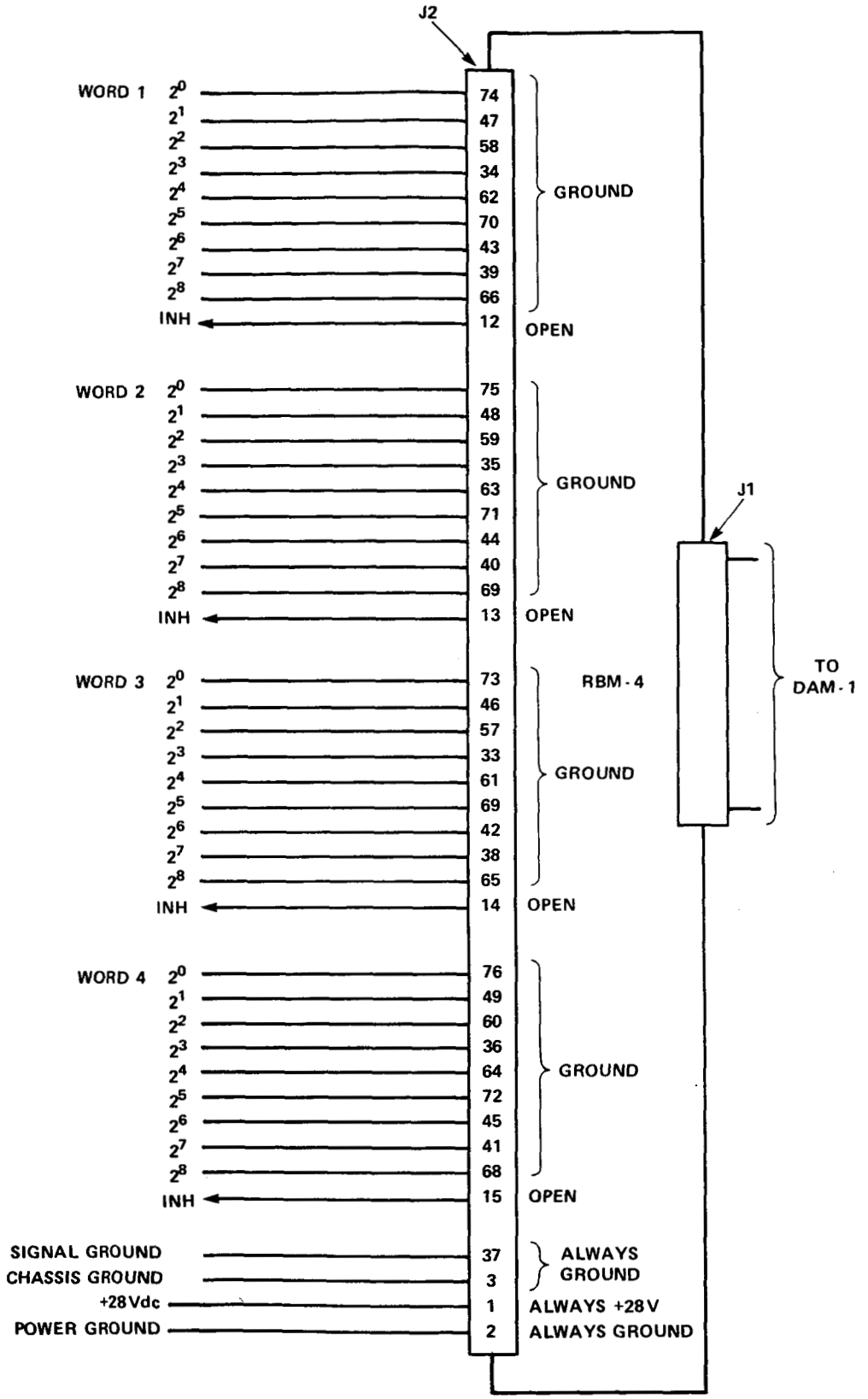


Figure C.14. RBM–4 Pin Assignments

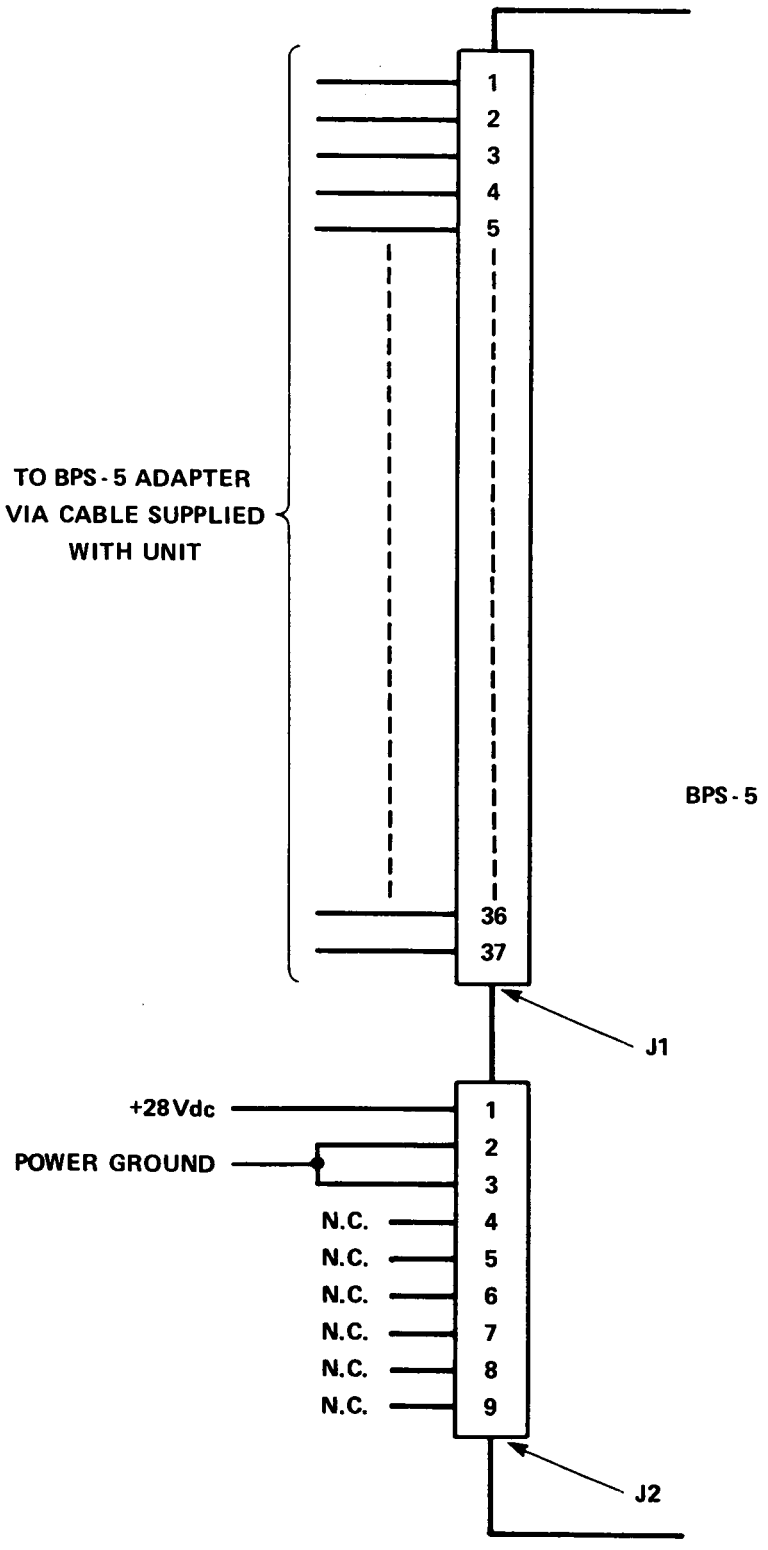


Figure C.15. BPS–5 Pin Assignments

APPENDIX D

EXPERIMENTER'S GROUND STATION INTERFACE CONNECTOR

APPENDIX D

EXPERIMENTER'S GROUND STATION INTERFACE CONNECTOR

The PCM Ground Station has available, for use by the experimenter, a connector containing parallel PCM data and appropriate timing signals. The connector is an Elco Type No. 30-8016-056-00-702, to which the experimenter should mate an Elco Type No. 30-8016-056-000-089. The pin assignments are as follows:

Pin Number	Function
A	Data 2^0
B	2^1
C	2^2
D	2^3
L	2^4
M	2^6
N	2^7
P	2^8
R	2^5
E, F, H, J, K, S, T, U	Ground
V	Clock
W	Frame
X	36-Bit
Y	Slo-Code

The data changes every 50μs (200μs for the 50kb system) and the data strobe signal CLOCK occurs after the data has settled. (See Figure D.1.) An accompanying FRAME signal can be used to identify the beginning of a frame, since the FRAME signal occurs simultaneously with the CHANNEL O DATA. Subframe decommutation can easily be accomplished by using a scheme such as the one shown in the block diagram in Figure D.2. The CLOCK signal is divided by sixteen to give a channel count (which is reset by the FRAME to maintain sync), and the subframe count is selected from the CHANNEL 1 DATA.

Noise problems are frequently encountered in the CLOCK line due to transitions in the data lines. A suggested noise-elimination circuit is shown in Figure D.3. The CLOCK is used to trigger a one-shot which then clocks the CLOCK into a flip-flop. Noise will trigger the one-shot, but will not get through the flip-flop.

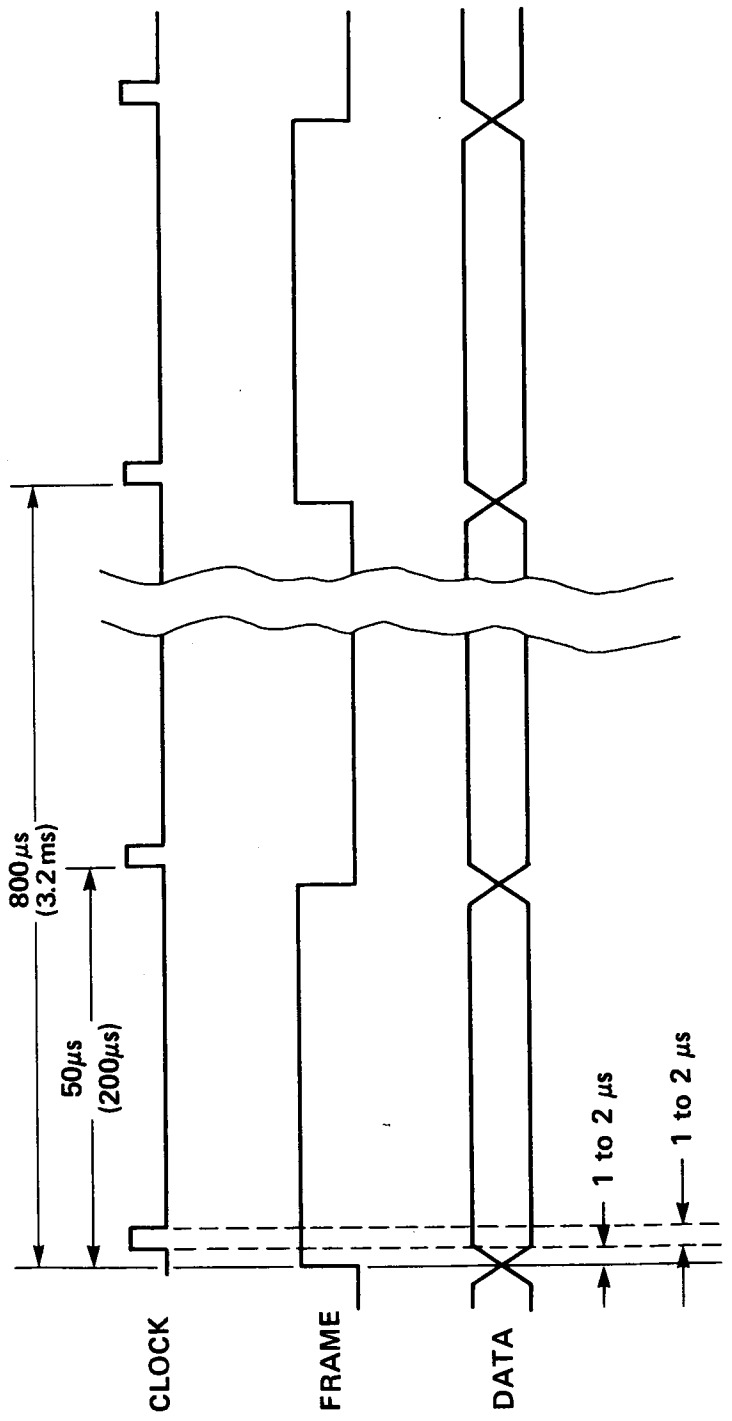
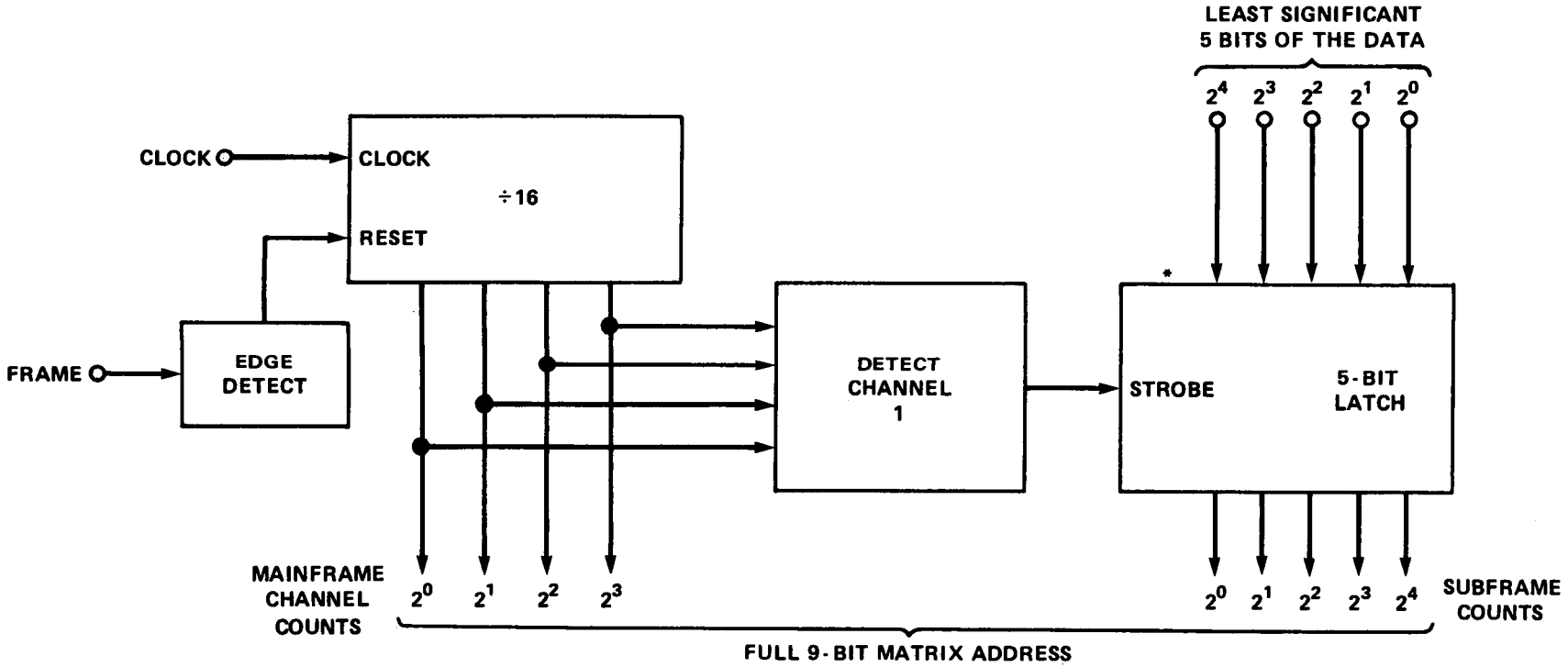


Figure D.1. Timing for 200kb (50kb) System



*NOTE: The least significant 5 bits of Channel 1 data has the subframe count, but it is backwards, i.e., - subframe count 2^4 is in data bit 2^0, etc. - Thus the reversal shown from input to output on the latch bits.

Figure D.2. Matrix Address Generation

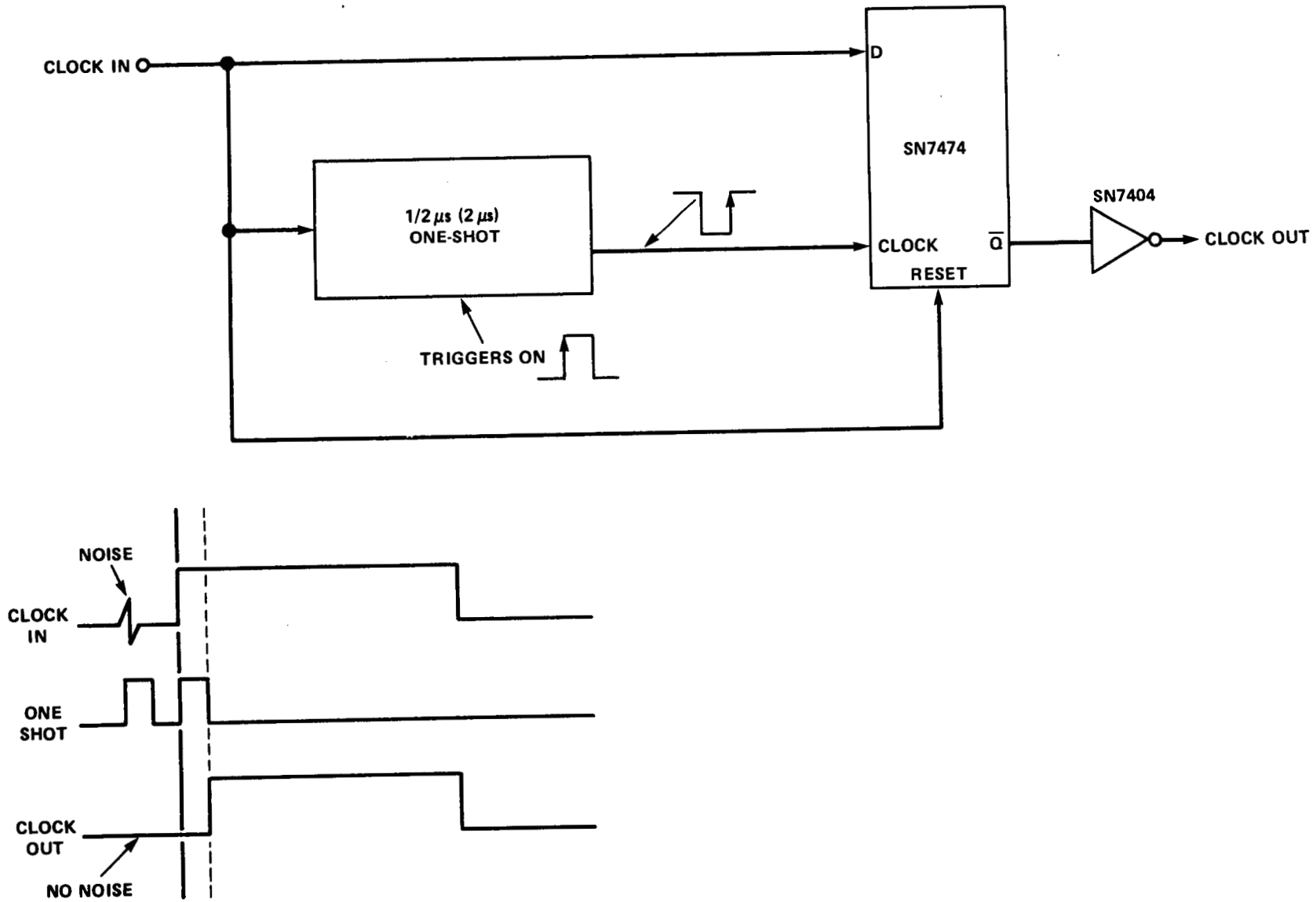


Figure D.3. Clock Noise Suppression

APPENDIX E

PCM EXPERIMENTER'S DATA TAPE

APPENDIX E

PCM EXPERIMENTER'S DATA TAPE

The final output of the PCM telemetry system is a standard 9-track computer tape. The experimenter will receive a copy of this tape if he requests it. The request form should be obtained from the instrumentation manager. A sample is shown in Figure E.1. Because this form requires "time of day" (not time from liftoff) as its base time, it is important that the form be completed at the launch site, following the launch, when the "time of day" for liftoff can be readily obtained from the ground station personnel. Filling out the form after everyone has returned from the field will frequently entail a tedious digging through records to find the recorded time of liftoff.

The format of the tape is shown in Figure E.2. For experimenters requiring a sample tape so that computer software can be prepared prior to the flight, there is a special PCM Sample Tape available from Code 743.4 (Hinds/Stattel). The sample tape is described in Appendix F.

Experimenters please note:

THIS IS A 9-TRACK, 800 BPI TAPE

It is the experimenter's responsibility to determine whether or not his computer system can handle this tape, and if not, to make his own arrangements to have a conversion performed to get the tape into a form useable by his system. Code 743.4 has only 9-track 800 BPI drives and cannot provide any other kind of tape. When the generating software on the Code 743.4 minicomputer determines that there are errors of any sort in the PCM data, a "flag" is inserted onto the tape. Positioning and meaning of these error codes are given in Figure E.3.

It should also be noted that the "P" bit in Figure E.2 is a parity error flag, not a parity bit. The 8 bytes of "header" information at the front of every record are there for use by a standard FORTRAN "V" format. The first record on the tape is an 80-byte "Flight ID" record, and it is also preceded by the 8-byte V-format information (88, blank, 84, blank) for that record.

Section 9.0 of this document contains a brief summary of the types of plots, listings, etc., which Code 743.4 can provide from the S9 tape. Further details of these capabilities is given in NASA X743-76-234.

The S9 tape will hold about 7 minutes of 200KBs PCM data (approximately 1/2 hour of 50KB's data). The experimenter should request however much data he really needs, of course, but if the necessary data is just barely over 7 minutes, it might be convenient for all concerned if the request could be kept to just under 7 minutes. If a second tape is necessary, it will normally be generated as a direct extension of the first tape. That is, the first time code on the second tape will be directly following the last time code of the first tape. The second tape will contain the header record (88 bytes) and the first tape of a 2-tape job will contain a file mark.

Experimenters experiencing any difficulty in reading or interpreting the S9 tapes should contact:

Ray Stattel (301) 982-5304 or 5287

ROCKET NO. 12.345

PCM DATA REDUCTION REQUEST

(SUBMIT TO CODE 743.4)

This form must be completed post-flight for any PCM telemetry links for which computer tapes are required. The requestor should determine the "time of day" on the ground station tape from which the computer tape is to be made. This should be done prior to leaving the launch site.

1. ROCKET NO.: 12.345

2. CARRIER FREQUENCY: 2258.9

3. LAUNCH TIME AS RECORDED ON FLIGHT TAPE

   MONTH JAN (01) DAY 22 YEAR 1976

   HOURS 8 MINUTES 45 SECONDS 01.181

4. DATA REDUCTION REQUIRED

   FROM: MINUTES 44 SECONDS 30

   TO: MINUTES 51 SECONDS 0

   (Above time to be expressed in "time-of-day", not as time-from-liftoff).

5. Unless a particular ground station tape is requested in this block, the computer tape(s) will be generated from whatever tape is first delivered to Code 743.4.

   VAB "A" VIDEO

6. Address to which computer tape(s) should be sent and phone number of person to be contacted if any questions arise concerning the data:

   John Experimenter 800/555-2020
   Dept of Confusion
   Univ of Podunk
   Podunk, Ohio
   12345

Figure E.1. Sample PCM Data Reduction Request (Page 1 of 2)

BALLOON EXPERIMENT_____

PCM DATA REDUCTION REQUEST
(SUBMIT TO CODE 743.4)

This form must be completed post-flight for any PCM telemetry links for which computer tapes are required. The requestor should determine the "time of day" on the ground station tape from which the computer tape is to be made. This should be done prior to leaving the launch site.

1. BALLOON EXPERIMENT: _____

2. CARRIER FREQUENCY: _____ MHz

3. LAUNCH TIME AS RECORDED ON FLIGHT TAPE:

   MONTH_____ DAY_____ YEAR_____

   HOURS_____ MINUTES_____ SECONDS_____

4. DATA REDUCTION REQUIRED

   FROM: HOURS_____ MINUTES_____ SECONDS_____

   TO: HOURS_____ MINUTES_____ SECONDS_____

   (Above time to be expressed in "time of day", NOT as time-from-liftoff).

5. Unless a particular ground station tape is requested in this block, the computer tape(s) will be generated from whatever tape is first delivered to Code 743.4.

6. Address to which computer tape(s) should be sent and phone number of person to be contacted if any questions arise concerning the data:

Figure E.1. Sample PCM Data Reduction Request (Page 2 of 2)

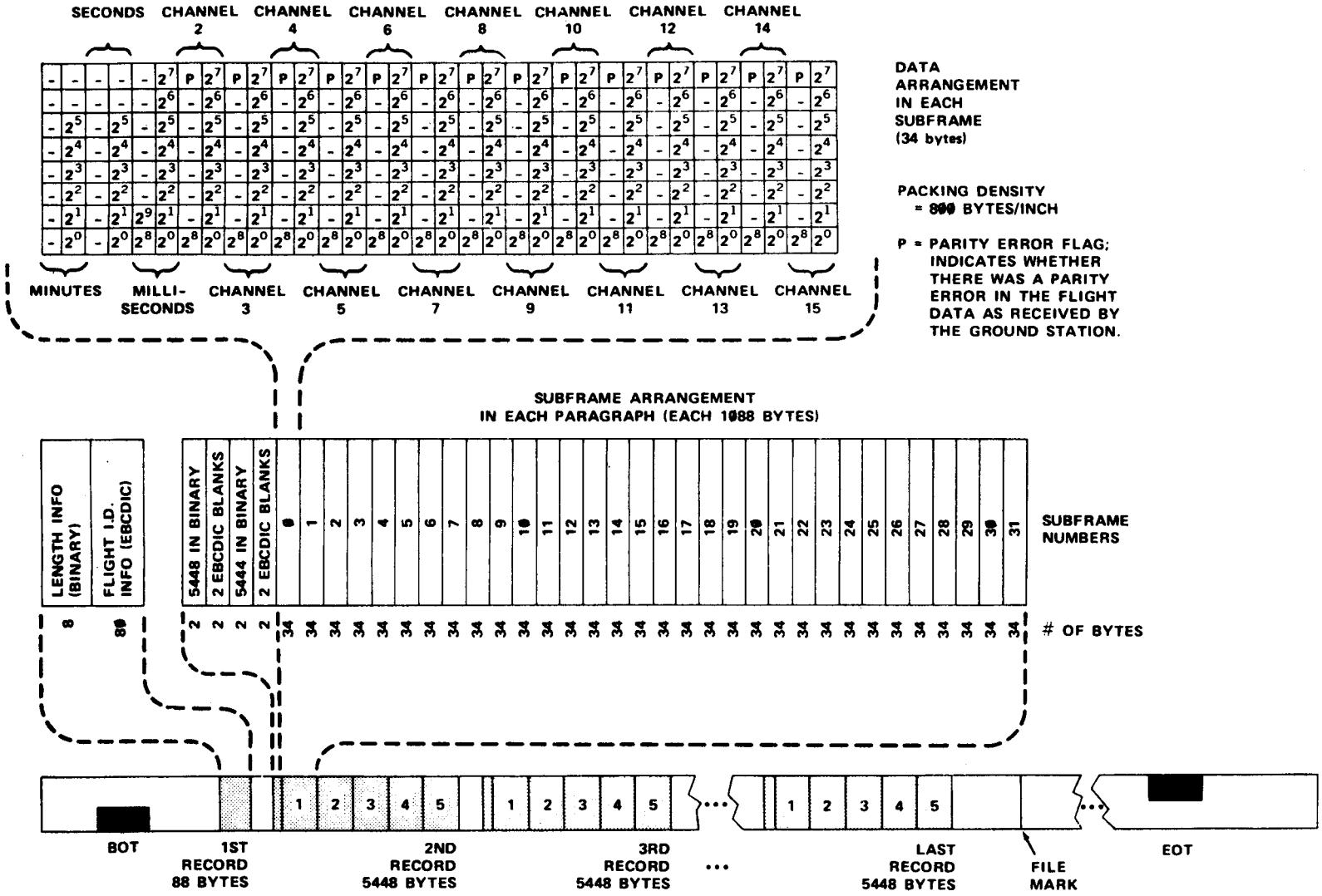


Figure E.2. Data Arrangement on the Form S9 Tape

FORM S9 ERROR CODES

All error codes indicate some kind of error concerning the main-frame sync code or the subframe sync code, and consequently all data is suspect for any frame that has an error flag. Surrounding frames are also mildly suspect, particularly in the case of the more severe error codes.

All error codes are put in the "minutes" word of a frame, and all are over 60 so they can be distinguished from valid time codes.

Error Code	Meaning & Severity
66	As a single, isolated code, this indicates a very mild error, namely a single suspect subframe sync code. Multiple 66 flags indicate that the subframe data may not even be associated with the correct subframe.
77	A fairly mild error flag indicating that there were bit errors in the frame-sync word for the flagged frame.
88	Very severe error code. Frame sync had bit errors and subframe sync is suspect. High probability of data errors.
99	A single 99 is a special code indicating that subframe sync has just been re-established after a period of being out of sync. If not surrounded by other error codes, this flag may be associated with other good data. Even a single 99, when followed by other flags makes the data highly suspect. Multiple 99 flags are the most severe error code because that indicates no data at all. That is, if a string of 99 flags appears, the data for all the associated frames must be ignored completely.

Figure E.3. Form S9 Error Codes

APPENDIX F

SAMPLE PCM TAPE

APPENDIX F

SAMPLE PCM TAPE

The Sounding Rocket Division (SRD) has a sample PCM data tape, which is available to experimenters who wish to develop computer programs to handle the data tapes produced by SRD's PCM system. This sample tape is 9 track and is in what SRD calls "S9" data format. This is the only type of PCM digital tape that SRD's PCM system will produce; 7 track tapes, etc., will not be produced at SRD.

The format of the S9 tape is shown in Figure E.1. Notice that each word on the tape contains a Parity Error Flag bit (indicated by the "P's" in the diagram), which if its value is 1 indicates that that data word was received by the PCM ground station with a parity error and is therefore suspect. On the sample tape, alternate "paragraphs" of data have been given alternate values for the Parity Error Flag.

The values of the sample data can be seen in Figure F.1. This figure shows, first of all, the header information that is contained in the 88 byte first tape record (shown schematically in Figure E.1). Below the header in Figure F.1 is a partial listing of the sample data in the first and last records on the tape. It is a partial listing of these records because the printout program omits Parity Error Flagged data from the printout. And since, as was mentioned above, alternate paragraphs of the sample tape have a Parity Error Flag on all of the data words in that paragraph, every other paragraph in the first and last sample tape records is missing from the printout.

As the sample data printed out in Figure F.1 suggests, the data in each position of each paragraph of the sample tape is simply the index of that data ~~word's position~~ within the paragraph (Ø-origin). This data pattern was produced by a simulator in order to make each data word in a paragraph uniquely identifiable.

Figure E.3, "Form S9 Error Codes," describes a set of error flags which, in addition to Parity Error Flags, might appear on an actual PCM data tape. The SRD sample tape contains data from a simulator and does not have any of these other error flags on it, because it contains no errors.

ROCKET NUMBER 12.345 PCM TELEMETRY TAPE PROCESSING
FIRING DATE 01 20 1976
LIFTOFF TIME IS 13HR, 19MIN, 00.000 SEC
TELEMETRY CARRIER FREQUENCY IS TEST

MIN	SECONDS	SUBFRAME	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	55.202	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	55.202	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31
18	55.203	2	34	35	36	37	38	39	40	41	42	43	44	45	46	47
18	55.204	3	50	51	52	53	54	55	56	57	58	59	60	61	62	63
18	55.205	4	66	67	68	69	70	71	72	73	74	75	76	77	78	79
18	55.206	5	82	83	84	85	86	87	88	89	90	91	92	93	94	95
18	55.206	6	98	99	100	101	102	103	104	105	106	107	108	109	110	111
18	55.207	7	114	115	116	117	118	119	120	121	122	123	124	125	126	127
18	55.208	8	130	131	132	133	134	135	136	137	138	139	140	141	142	143
18	55.209	9	146	147	148	149	150	151	152	153	154	155	156	157	158	159
18	55.210	10	162	163	164	165	166	167	168	169	170	171	172	173	174	175
18	55.210	11	178	179	180	181	182	183	184	185	186	187	188	189	190	191
18	55.211	12	194	195	196	197	198	199	200	201	202	203	204	205	206	207
18	55.212	13	210	211	212	213	214	215	216	217	218	219	220	221	222	223
18	55.213	14	226	227	228	229	230	231	232	233	234	235	236	237	238	239
18	55.214	15	242	243	244	245	246	247	248	249	250	251	252	253	254	255
18	55.214	16	258	259	260	261	262	263	264	265	266	267	268	269	270	271
18	55.215	17	274	275	276	277	278	279	280	281	282	283	284	285	286	287
18	55.216	18	290	291	292	293	294	295	296	297	298	299	300	301	302	303
18	55.217	19	306	307	308	309	310	311	312	313	314	315	316	317	318	319
18	55.218	20	322	323	324	325	326	327	328	329	330	331	332	333	334	335
18	55.218	21	338	339	340	341	342	343	344	345	346	347	348	349	350	351
18	55.219	22	354	355	356	357	358	359	360	361	362	363	364	365	366	367
18	55.220	23	370	371	372	373	374	375	376	377	378	379	380	381	382	383
18	55.221	24	386	387	388	389	390	391	392	393	394	395	396	397	398	399
18	55.222	25	402	403	404	405	406	407	408	409	410	411	412	413	414	415
18	55.222	26	418	419	420	421	422	423	424	425	426	427	428	429	430	431
18	55.223	27	434	435	436	437	438	439	440	441	442	443	444	445	446	447
18	55.224	28	450	451	452	453	454	455	456	457	458	459	460	461	462	463
18	55.225	29	466	467	468	469	470	471	472	473	474	475	476	477	478	479
18	55.226	30	482	483	484	485	486	487	488	489	490	491	492	493	494	495
18	55.226	31	498	499	500	501	502	503	504	505	506	507	508	509	510	511
18	55.227	0														
18	55.228	1														
18	55.229	2														
18	55.230	3														
18	55.230	4														
18	55.231	5														
18	55.232	6														
18	55.233	7														
18	55.234	8														
18	55.234	9														
18	55.235	10														
18	55.236	11														
18	55.237	12														
18	55.238	13														
18	55.238	14														
18	55.239	15														
18	55.240	16														
18	55.241	17														
18	55.242	18														
18	55.242	19														
18	55.243	20														
18	55.244	21														
18	55.245	22														
18	55.246	23														
18	55.246	24														
18	55.247	25														
18	55.248	26														
18	55.249	27														
18	55.250	28														
18	55.250	29														
18	55.251	30														
18	55.252	31														
18	55.253	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	55.254	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31
18	55.254	2	34	35	36	37	38	39	40	41	42	43	44	45	46	47
18	55.255	3	50	51	52	53	54	55	56	57	58	59	60	61	62	63
18	55.256	4	66	67	68	69	70	71	72	73	74	75	76	77	78	79
18	55.257	5	82	83	84	85	86	87	88	89	90	91	92	93	94	95
18	55.258	6	98	99	100	101	102	103	104	105	106	107	108	109	110	111
18	55.258	7	114	115	116	117	118	119	120	121	122	123	124	125	126	127
18	55.259	8	130	131	132	133	134	135	136	137	138	139	140	141	142	143
18	55.260	9	146	147	148	149	150	151	152	153	154	155	156	157	158	159
18	55.261	10	162	163	164	165	166	167	168	169	170	171	172	173	174	175
18	55.262	11	178	179	180	181	182	183	184	185	186	187	188	189	190	191
18	55.262	12	194	195	196	197	198	199	200	201	202	203	204	205	206	207
18	55.263	13	210	211	212	213	214	215	216	217	218	219	220	221	222	223
18	55.264	14	226	227	228	229	230	231	232	233	234	235	236	237	238	239
18	55.265	15	242	243	244	245	246	247	248	249	250	251	252	253	254	255
18	55.266	16	258	259	260	261	262	263	264	265	266	267	268	269	270	271
18	55.266	17	274	275	276	277	278	279	280	281	282	283	284	285	286	287
18	55.267	18	290	291	292	293	294	295	296	297	298	299	300	301	302	303
18	55.268	19	306	307	308	309	310	311	312	313	314	315	316	317	318	319
18	55.269	20	322	323	324	325	326	327	328	329	330	331	332	333	334	335
18	55.270	21	338	339	340	341	342	343	344	345	346	347	348	349	350	351
18	55.270	22	354	355	356	357	358	359	360	361	362	363	364	365	366	367
18	55.271	23	370	371	372	373	374	375	376	377	378	379	380	381	382	383
18	55.272	24	386	387	388	389	390	391	392	393	394	395	396	397	398	399
18	55.273	25	402	403	404	405	406	407	408	409	410	411	412	413	414	415
18	55.274	26	418	419	420	421	422	423	424	425	426	427	428	429	430	431
18	55.274	27	434	435	436	437	438	439	440	441	442	443	444	445	446	447
18	55.275	28	450	451	452	453	454	455	456	457	458	459	460	461	462	463
18	55.276	29	466	467	468	469	470	471	472	473	474	475	476	477	478	479
18	55.277	30	482	483	484	485	486	487	488	489	490	491	492	493	494	495
18	55.278	31	498	499	500	501	502	503	504	505	506	507	508	509	510	511
18	55.278	0														
18	55.279	1														
18	55.280	2														
18	55.281	3														
18	55.282	4														
18	55.282	5														
18	55.283	6														
18	55.284	7														
18	55.285	8														
18	55.286	9														
18	55.286	10														
18	55.287	11														
18	55.288	12														
18	55.289	13														
18	55.290	14														
18	55.290	15														
18	55.291	16														
18	55.292	17														
18	55.293	18														
18	55.294	19														
18	55.294	20														
18	55.295	21														
18	55.296	22														
18	55.297	23														
18	55.298	24														
18	55.298	25														
18	55.299	26														
18	55.300	27														
18	55.301	28														
18	55.302	29														
18	55.302	30														
18	55.303	31														
18	55.304	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	55.305	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31
18	55.306	2	34	35	36	37	38	39	40	41	42	43	44	45	46	47
18	55.306	3	50	51	52	53	54	55	56	57	58	59	60	61	62	63
18	55.307	4	66	67	68	69	70	71	72	73	74	75	76	77	78	79
18	55.308	5	82	83	84	85	86	87	88	89	90	91	92	93	94	95
18	55.309	6	98	99	100	101	102	103	104	105	106	107	108	109	110	111
18	55.310	7	114	115	116	117	118	119	120	121	122	123	124	125	126	127
18	55.310	8	130	131	132	133	134	135	136	137	138	139	140	141	142	143
18	55.311	9	146	147	148	149	150	151	152	153	154	155	156	157	158	159
18	55.312	10	162	163	164	165	166	167	168	169	170	171	172	173	174	175
18	55.313	11	178	179	180	181	182	183	184	185	186	187	188	189	190	191
18	55.314	12	194	195	196	197	198	199	200	201	202	203	204	205	206	207
18	55.314	13	210	211	212	213	214	215	216	217	218	219	220	221	222	223
18	55.315	14	226	227	228	229	230	231	232	233	234	235	236	237	238	239
18	55.316	15	242	243	244	245	246	247	248	249	250	251	252	253	254	255
18	55.317	16	258	259	260	261	262	263	264	265	266	267	268	269	270	271
18	55.318	17	274	275	276	277	278	279	280	281	282	283	284	285	286	287
18	55.318	18	290	291	292	293	294	295	296	297	298	299	300	301	302	303
18	55.319	19	306	307	308	309	310	311	312	313	314	315	316	317	318	319
18	55.320	20	322	323	324	325	326	327	328	329	330	331	332	333	334	335
18	55.321	21	338	339	340	341	342	343	344	345	346	347	348	349	350	351
18	55.322	22	354	355	356	357	358	359	360	361	362	363	364	365	366	367
18	55.322	23	370	371	372	373	374	375	376	377	378	379	380	381	382	383
18	55.323	24	386	387	388	389	390	391	392	393	394	395	396	397	398	399
18	55.324	25	402	403	404	405	406	407	408	409	410	411	412	413	414	415
18	55.325	26	418	419	420	421	422	423	424	425	426	427	428	429	430	431
18	55.326	27	434	435	436	437	438	439	440	441	442	443	444	445	446	447
18	55.326	28	450	451	452	453	454	455	456	457	458	459	460	461	462	463
18	55.327	29	466	467	468	469	470	471	472	473	474	475	476	477	478	479
18	55.328	30	482	483	484	485	486	487	488	489	490	491	492	493	494	495
18	55.329	31	498	499	500	501	502	503	504	505	506	507	508	509	510	511

Figure F.1. TAPECK Printout of the Sample PCM Tape (Page 1 of 2)

MIN	SECONDS	SUBFRAME	2	3	4	5	6	7	8	9	10	11	12	13	14	15
19	5.186	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
19	5.187	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31
19	5.187	2	34	35	36	37	38	39	40	41	42	43	44	45	46	47
19	5.188	3	50	51	52	53	54	55	56	57	58	59	60	61	62	63
19	5.189	4	66	67	68	69	70	71	72	73	74	75	76	77	78	79
19	5.190	5	82	83	84	85	86	87	88	89	90	91	92	93	94	95
19	5.191	6	98	99	100	101	102	103	104	105	106	107	108	109	110	111
19	5.191	7	114	115	116	117	118	119	120	121	122	123	124	125	126	127
19	5.192	8	130	131	132	133	134	135	136	137	138	139	140	141	142	143
19	5.193	9	146	147	148	149	150	151	152	153	154	155	156	157	158	159
19	5.194	10	162	163	164	165	166	167	168	169	170	171	172	173	174	175
19	5.195	11	178	179	180	181	182	183	184	185	186	187	188	189	190	191
19	5.195	12	194	195	196	197	198	199	200	201	202	203	204	205	206	207
19	5.196	13	210	211	212	213	214	215	216	217	218	219	220	221	222	223
19	5.197	14	226	227	228	229	230	231	232	233	234	235	236	237	238	239
19	5.198	15	242	243	244	245	246	247	248	249	250	251	252	253	254	255
19	5.199	16	258	259	260	261	262	263	264	265	266	267	268	269	270	271
19	5.199	17	274	275	276	277	278	279	280	281	282	283	284	285	286	287
19	5.200	18	290	291	292	293	294	295	296	297	298	299	300	301	302	303
19	5.201	19	306	307	308	309	310	311	312	313	314	315	316	317	318	319
19	5.202	20	322	323	324	325	326	327	328	329	330	331	332	333	334	335
19	5.203	21	338	339	340	341	342	343	344	345	346	347	348	349	350	351
19	5.203	22	354	355	356	357	358	359	360	361	362	363	364	365	366	367
19	5.204	23	370	371	372	373	374	375	376	377	378	379	380	381	382	383
19	5.205	24	386	387	388	389	390	391	392	393	394	395	396	397	398	399
19	5.206	25	402	403	404	405	406	407	408	409	410	411	412	413	414	415
19	5.207	26	418	419	420	421	422	423	424	425	426	427	428	429	430	431
19	5.207	27	434	435	436	437	438	439	440	441	442	443	444	445	446	447
19	5.208	28	450	451	452	453	454	455	456	457	458	459	460	461	462	463
19	5.209	29	466	467	468	469	470	471	472	473	474	475	476	477	478	479
19	5.210	30	482	483	484	485	486	487	488	489	490	491	492	493	494	495
19	5.211	31	498	499	500	501	502	503	504	505	506	507	508	509	510	511
19	5.211	0														
19	5.212	1														
19	5.213	2														
19	5.214	3														
19	5.215	4														
19	5.215	5														
19	5.216	6														
19	5.217	7														
19	5.218	8														
19	5.219	9														
19	5.219	10														
19	5.220	11														
19	5.221	12														
19	5.222	13														
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19	5.223	15														
19	5.224	16														
19	5.225	17														
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19	5.227	19														
19	5.227	20														
19	5.228	21														
19	5.229	22														
19	5.230	23														
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19	5.231	25														
19	5.232	26														
19	5.233	27														
19	5.234	28														
19	5.235	29														
19	5.235	30														
19	5.236	31														
19	5.237	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
19	5.238	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31
19	5.239	2	34	35	36	37	38	39	40	41	42	43	44	45	46	47
19	5.239	3	50	51	52	53	54	55	56	57	58	59	60	61	62	63
19	5.240	4	66	67	68	69	70	71	72	73	74	75	76	77	78	79
19	5.241	5	82	83	84	85	86	87	88	89	90	91	92	93	94	95
19	5.242	6	98	99	100	101	102	103	104	105	106	107	108	109	110	111
19	5.243	7	114	115	116	117	118	119	120	121	122	123	124	125	126	127
19	5.243	8	130	131	132	133	134	135	136	137	138	139	140	141	142	143
19	5.244	9	146	147	148	149	150	151	152	153	154	155	156	157	158	159
19	5.245	10	162	163	164	165	166	167	168	169	170	171	172	173	174	175
19	5.246	11	178	179	180	181	182	183	184	185	186	187	188	189	190	191
19	5.247	12	194	195	196	197	198	199	200	201	202	203	204	205	206	207
19	5.247	13	210	211	212	213	214	215	216	217	218	219	220	221	222	223
19	5.248	14	226	227	228	229	230	231	232	233	234	235	236	237	238	239
19	5.249	15	242	243	244	245	246	247	248	249	250	251	252	253	254	255
19	5.250	16	258	259	260	261	262	263	264	265	266	267	268	269	270	271
19	5.251	17	274	275	276	277	278	279	280	281	282	283	284	285	286	287
19	5.251	18	290	291	292	293	294	295	296	297	298	299	300	301	302	303
19	5.252	19	306	307	308	309	310	311	312	313	314	315	316	317	318	319
19	5.253	20	322	323	324	325	326	327	328	329	330	331	332	333	334	335
19	5.254	21	338	339	340	341	342	343	344	345	346	347	348	349	350	351
19	5.255	22	354	355	356	357	358	359	360	361	362	363	364	365	366	367
19	5.255	23	370	371	372	373	374	375	376	377	378	379	380	381	382	383
19	5.256	24	386	387	388	389	390	391	392	393	394	395	396	397	398	399
19	5.257	25	402	403	404	405	406	407	408	409	410	411	412	413	414	415
19	5.258	26	418	419	420	421	422	423	424	425	426	427	428	429	430	431
19	5.259	27	434	435	436	437	438	439	440	441	442	443	444	445	446	447
19	5.259	28	450	451	452	453	454	455	456	457	458	459	460	461	462	463
19	5.260	29	466	467	468	469	470	471	472	473	474	475	476	477	478	479
19	5.261	30	482	483	484	485	486	487	488	489	490	491	492	493	494	495
19	5.262	31	498	499	500	501	502	503	504	505	506	507	508	509	510	511
19	5.263	0														
19	5.263	1														
19	5.264	2														
19	5.265	3														
19	5.266	4														
19	5.267	5														
19	5.267	6														
19	5.268	7														
19	5.269	8														
19	5.270	9														
19	5.271	10														
19	5.271	11														
19	5.272	12														
19	5.273	13														
19	5.274	14														
19	5.275	15														
19	5.275	16														
19	5.276	17														
19	5.277	18														
19	5.278	19														
19	5.279	20														
19	5.279	21														
19	5.280	22														
19	5.281	23														
19	5.282	24														
19	5.283	25														
19	5.283	26														
19	5.284	27														
19	5.285	28														
19	5.286	29														
19	5.287	30														
19	5.287	31														
19	5.288	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15
19	5.289	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31
19	5.290	2	34	35	36	37	38	39	40	41	42	43	44	45	46	47
19	5.291	3	50	51	52	53	54	55	56	57	58	59	60	61	62	63
19	5.291	4	66	67	68	69	70	71	72	73	74	75	76	77	78	79
19	5.292	5	82	83	84	85	86	87	88	89	90	91	92	93	94	95
19	5.293	6	98	99	100	101	102	103	104	105	106	107	108	109	110	111
19	5.294	7	114	115	116	117	118	119	120	121	122	123	124	125	126	127
19	5.295	8	130	131	132	133	134	135	136	137	138	139	140	141	142	143
19	5.295	9	146	147	148	149	150	151	152	153	154	155	156	157	158	159
19	5.296	10	162	163	164	165	166	167	168	169	170	171	172	173	174	175
19	5.297	11	178	179	180	181	182	183	184	185	186	187	188	189	190	191
19	5.298	12	194	195	196	197	198	199	200	201	202	203	204	205	206	207
19	5.299	13	210	211	212	213	214	215	216	217	218	219	220	221	222	223
19	5.299	14	226	227	228	229	230	231	232	233	234	235	236	237	238	239
19	5.300	15	242	243	244	245	246	247	248	249	250	251	252	253	254	255
19	5.301	16	258	259	260	261	262	263	264	265	266	267	268	269	270	271
19	5.302	17	274	275	276	277	278	279	280	281	282	283	284	285	286	287
19	5.303	18	290	291	292	293	294	295	296	297	298	299	300	301	302	303
19	5.303	19	306	307	308	309	310	311	312	313	314	315	316	317	318	319
19	5.304	20	322	323	324	325	326	327	328	329	330	331	332	333	334	335
19	5.305	21	338	339	340	341	342	343	344	345	346	347	348	349	350	351
19	5.306	22	354	355	356	357	358	359	360	361	362	363	364	365	366	367
19	5.307	23	370	371	372	373	374	375	376	377	378	379	380	381	382	383
19	5.307	24	386	387	388	389	390	391	392	393	394	395	396	397	398	399
19	5.308	25	402	403	404	405	406	407	408	409	410	411	412	413	414	415
19	5.309	26	418	419	420	421	422	423	424	425	426	427	428	429	430	431
19	5.310	27	434	435	436	437	438	439	440	441	442	443	444	445	446	447
19	5.311	28	450	451	452	453	454	455	456	457	458	459	460	461	462	463
19	5.311	29	466	467	468	469	470	471	472	473	474	475	476	477	478	479
19	5.312	30	482	483	484	485	486	487	488	489	490	491	492	493	494	495
19	5.313	31	498	499	500	501	502	503	504	505	506	507	508	509	510	511

PE = 0
TE = 0
66 = 0
77 = 0
88 = 0
99 = 0

Figure F.1. TAPECK Printout of the Sample PCM Tape (Page 2 of 2)